



2.4 GHz wake-up receiver with suppressed substrate noise coupling

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Abstract

The switching noise generated in digital circuits propagates through conductive silicon substrate to analog circuits in a mixed-signal CMOS LSI. Substrate noise coupling may degrade the performance of the analog circuits, and may result in a fault operation of the mixed-signal LSI in the worst-case. In this paper, the substrate noise coupling between the clock recovery circuit and the input port of the envelop detector in a low-power wake-up receiver (WuRx) was investigated experimentally. The propagation path of the substrate noise coupling was clarified by comparing the experimental results with the circuit simulations on the basis of an equivalent circuit model. The design of the WuRx was modified on the basis of the findings to suppress the substrate noise coupling. The fabricated WuRx successfully operated a 100-kbps PWM signal with a carrier frequency of 2.4 GHz, and the effectiveness of the noise coupling suppression recipe was confirmed.

Keywords Wake-up receiver · Mixed signal · Analog and digital · Substrate noise coupling · Clock and data recovery

1 Introduction

Reducing power consumption in sensor nodes is a key issue in the development of the Internet-of-Things. A candidate to achieve low power consumption is a wake-up radio. A wake-up receiver (WuRx) continuously monitors the wireless-communication channel for receiving communication requests from other sensor nodes. When the WuRx receives a communication request, it activates other parts of the sensor node for sensing, data processing, and data transmission. When not activated, these parts remain in sleep mode to save the power consumption. Many kinds of WuRx with wireless carrier frequencies from 0.9 to 60 GHz have been reported [1–7].

In the microwave and millimeter-wave regions, input impedance matching is essential. When the input characteristic impedance of an analog frontend circuit does not match the characteristic impedance of the transmission line connected to the antenna in wireless equipment, the RF power input to the analog frontend circuit is reflected and the effective input power is reduced. Several kinds of

impedance matching technique are used in the microwave and millimeter-wave regions. In hybrid integration systems, bulk acoustic wave (BAW) and surface acoustic wave (SAW) filters are good candidates for RF input [2]. On the other hand, an impedance matching circuit monolithically integrated with CMOS IC is desired to reduce the cost and size of sensor nodes. In millimeter-wave regions, like 60 GHz, a microstrip line with a bottom-layer metal for the ground plane and a top-layer metal for the signal line is commonly used in the impedance matching circuit [5]. In the microwave region, a microstrip line becomes unrealistically long and on-chip spiral inductors are used to reduce the chip sizes of CMOS ICs [3, 4, 6]. A usual spiral inductor is composed of a top-layer metal without a lower-layer metal for the ground plane because the Eddy current flowing in the lower-layer metal degrades the quality factor of the inductor.

When the logic levels of nodes in CMOS digital circuits (i.e. clock and data recovery circuit in WuRx) switch, the electric potential of the silicon substrate changes due to the capacitive coupling between the drains of MOSFETs and the substrate. The potential change propagates to the analog frontend circuit through the substrate and acts as “noise” [8, 9]. The noise fluctuates the threshold voltages of MOSFETs (back-gate effect) in the analog circuits. This is a critical issue for the analog circuits, especially those operating near the threshold voltage to achieve very low

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power consumption. The substrate noise coupling also has an impact on the electric potential in the analog input port. While the signal line in the microstrip structure of the impedance matching circuit is shielded from the silicon substrate by means of the bottom-layer metal, the electric potentials of spiral inductors and metal–insulator–metal (MIM) capacitors may be influenced by the substrate noise through the capacitive coupling [10].

In this paper, the substrate noise coupling between the digital circuit and the input port of the envelop detector in a previously fabricated 2.4-GHz WuRx was investigated experimentally. The propagation path of the substrate noise coupling was clarified by comparing the experimental results with the circuit simulations on the basis of an equivalent circuit model. A modified version of a WuRx to suppress the substrate noise coupling was designed and fabricated. The experimental results for the fabricated WuRx confirmed the effectiveness of the noise coupling suppression recipe.

2 Evaluation of substrate noise coupling

Figure 1 illustrates the block diagram of the WuRx used for investigating the substrate coupling noise. The WuRx was fabricated by using 0.18- μm mixed signal/RF CMOS process with one poly and six metal layers. It consisted of an impedance matching circuit, an envelope detector, high-gain baseband amplifiers, and a clock and data recovery (CDR) circuit. Two spiral inductors and one MIM capacitor were employed in the impedance matching circuit. The envelope detector and baseband amplifiers had the same circuit configuration. The detector operated at around the subthreshold voltage of the MOSFET M1. The detection scheme was based on the nonlinearity of drain current in

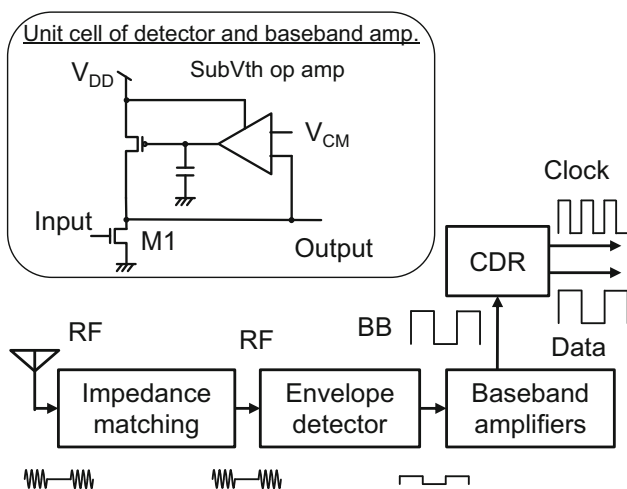


Fig. 1 Block diagram of WuRx

the operation bias [4, 5]. The high-gain baseband amplifiers and detector canceled a DC offset with a subthreshold-operated operational amplifier (subVth op amp) operating as a feedback circuit [11]. The feedback circuit fixed the voltages of the input and output ports of the subVth op amp to common-mode voltage V_{CM} in a low-frequency region to DC. The high-gain baseband amplifiers comprised two parts of the unit cell shown in Fig. 1. The CDR used an injection locked oscillator (ILO) for clock recovery [5]. While the ILO synchronized to the input baseband signal of non-return-to-zero (NRZ) data detected and amplified in the preceding circuits, it was free-running without an input baseband signal. The baseband NRZ data with reduced timing jitter was obtained by latching the baseband signal with a D-type flip/flop and recovered clock.

Figure 2 shows the circuit configuration of the impedance matching circuit, bias circuit, and envelop detector. The input port I_{DET} was connected to an external current source for simultaneously biasing the gate of MOSFET M1 and the common-mode voltage V_{CM} of the subVth op amp. The voltage fluctuations of the RF input port (RF_{in}) and I_{DET} in the WuRx were measured with a spectrum analyzer when the detector and high-gain amplifiers were turned off and the ILO was free-running. Figure 3 shows the measured spectrum of the detector input port along with that of the free-running clock. A clear coupling of -73 dB between the clock output and I_{DET} was observed, while the voltage fluctuation of RF_{in} was smaller than the noise floor of the spectrum analyzer. Since the designed value of total gain of the detector and high-gain baseband amplifiers was about 100 dB, a positive feedback loop could be formed. This might result in unwanted oscillation. No correct operation was obtained for the WuRx when the detector and high-gain amplifiers were turned on. To further investigate the coupling between the clock output port and I_{DET} , a square wave with a voltage swing of 1.5 V and a repetition rate of 377 kHz was applied to the clock output port while the WuRx was turned off. Figure 4 shows the waveforms of I_{DET} and the applied square wave observed

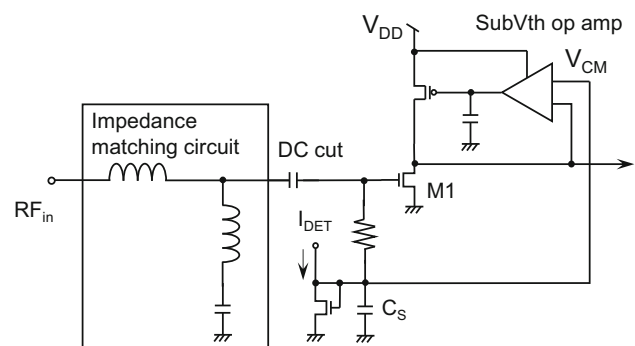


Fig. 2 Circuit configuration of impedance matching circuit, bias circuit, and envelop detector

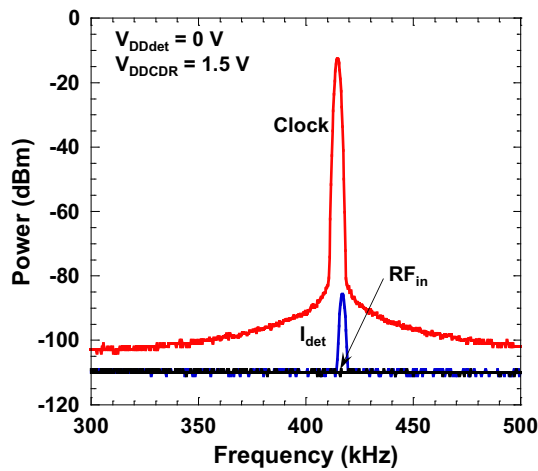
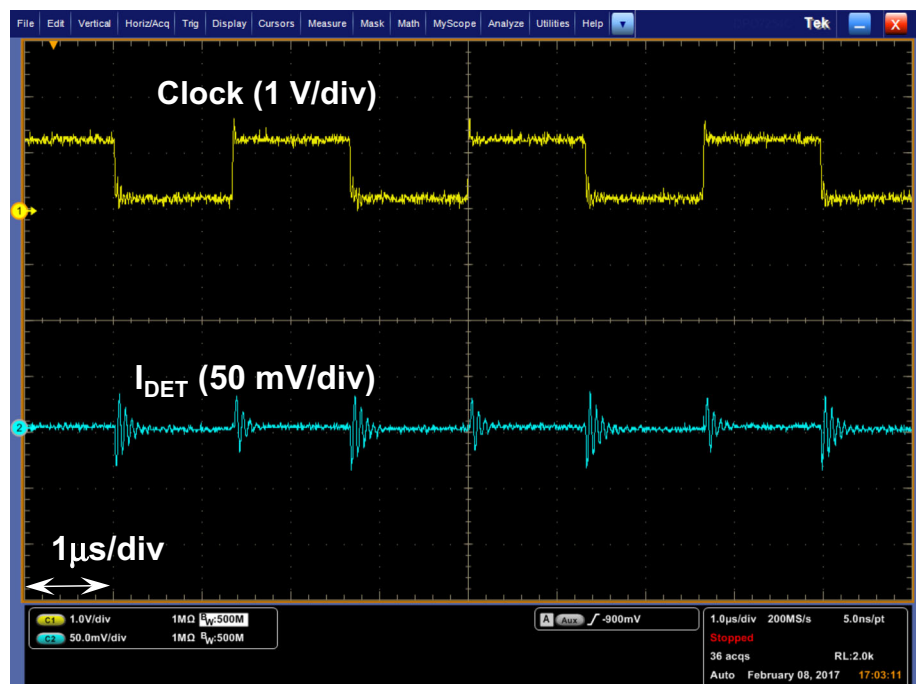


Fig. 3 Measured spectra of detector input port and free-running clock

with an oscilloscope. The waveform of I_{DET} differentiated from the applied square wave, followed by some ringing wave.

The measured results were compared with circuit simulations to explore the coupling between the clock output port and I_{DET} . Figure 5 shows the schematic circuit model for the simulations. The equivalent circuit models of the spiral inductors and MIM capacitors with parasitic elements were provided by the foundry. The contact resistances of the guard rings and MOSFETs to the substrate were calculated with an elliptic approximation [12, 13]. Figure 6 shows the simulated waveforms at I_{DET} and the clock output port, corresponding to those shown in Fig. 4. The circuit simulations revealed that the main coupling

Fig. 4 Waveforms of input port I_{DET} and applied square wave



path between the clock output port and the input port I_{DET} was from the MOSFET drains in the clock output buffer to MIM capacitor C_S shown in Fig. 5 through the parasitic capacitances and the substrate resistance. Generic logic MOSFETs were used in the clock output buffer and the CDR circuit, and the MIM capacitor C_S was placed next to the clock output buffer.

3 Modified design

We modified the design of the WuRx on the basis of the findings described in the previous section to suppress the substrate noise coupling. The baseband signal format was changed from NRZ to pulse-width modulation (PWM). In accordance with the signal format, a clock recovery circuit for the PWM signal [4] was used. Since the repetition frequency of a ring oscillator in the clock recovery circuit was one-order higher than that of baseband signal frequency [4], the gain of the baseband amplifier was decreased at the repetition frequency of the ring oscillator. Generic logic MOSFETs in the data and clock buffers were replaced by deep N-well (DNW) RF MOSFETs, and microstrip lines were used between the CDR circuit and output buffers to reduce the noise current injection to the substrate. The capacitance value of C_S was decreased from 10 to 1 pF to reduce the parasitic capacitance between the MIM capacitor and the substrate. The CDR circuit was surrounded by a grounded DNW guard ring to reduce the

Fig. 5 Schematic circuit model for simulating substrate noise coupling

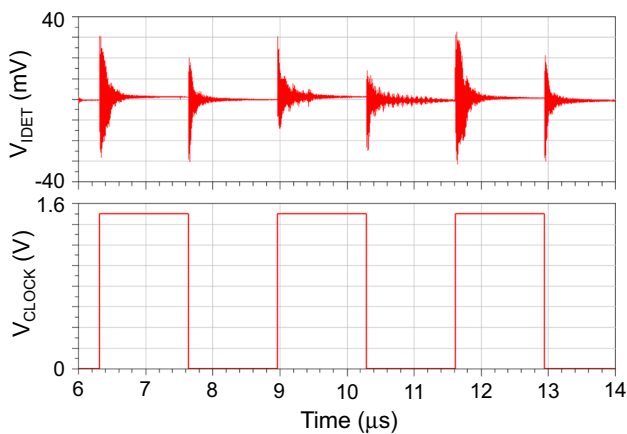
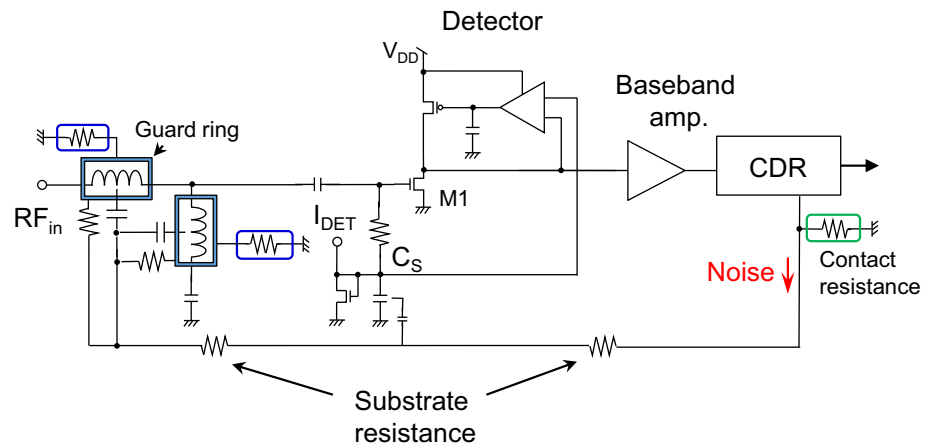


Fig. 6 Simulated waveforms of input port I_{DET} and clock output port

noise current injection [14], and only one spiral inductor was used in the impedance matching circuit.

4 Experimental results

A modified version of the WuRx was fabricated with the same CMOS process as the previous version. Figure 7 shows a microphotograph of the fabricated WuRx. The fabricated WuRx was measured with RF and power-supply probes on a chip. The logic “1” and “0” in the PWM format were defined as pulses with duty ratios of 75 and 25%, respectively. A NRZ-to-PWM converter was fabricated with commercially available logic ICs based on the definition. A 2.4-GHz continuous wave (CW) was modulated with the PWM baseband signal converted from a NRZ pseudo-random bit stream, and input to the WuRx. Figure 8 shows the measured waveforms. The uppermost wave was a 100-kbps PWM baseband signal used to modulate 2.4-GHz CW. Successful recovery of NRZ data and clock from a PWM-modulated signal with power of

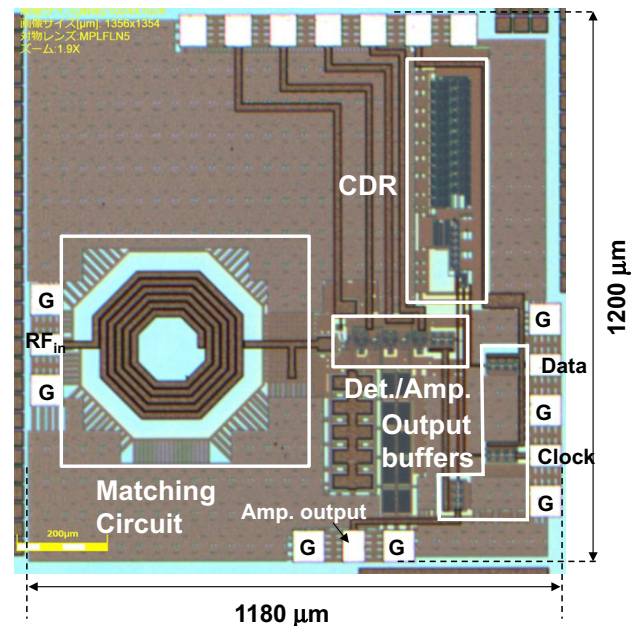


Fig. 7 Microphotograph of fabricated WuRx

– 30 dBm was achieved. Sensitivity of our circuit at a bit error rate (BER) of 10^{-3} was – 32 dBm. Also, the sensitivity estimated from noise and conversion efficiency [1] is given to

$$Sensitivity = \frac{3.5 \sqrt{\int N(f) df}}{\gamma}, \quad (1)$$

where $N(f)$ is noise power density, and γ is conversion efficiency [output voltage/input power (V/W)]. The calculated sensitivity using Eq. (1) was – 46 dBm. We consider that the reason why the BER degraded is due to noise of the measurement setup. The power consumption of the detector and baseband amplifiers was $11.3 \mu\text{W}$, while that of the CDR circuit including data and clock output buffers was $83.7 \mu\text{W}$.

Fig. 8 Measured waveforms of 100-kbps PWM baseband signal used to modulate 2.4-GHz CW, recovered NRZ data, and clock

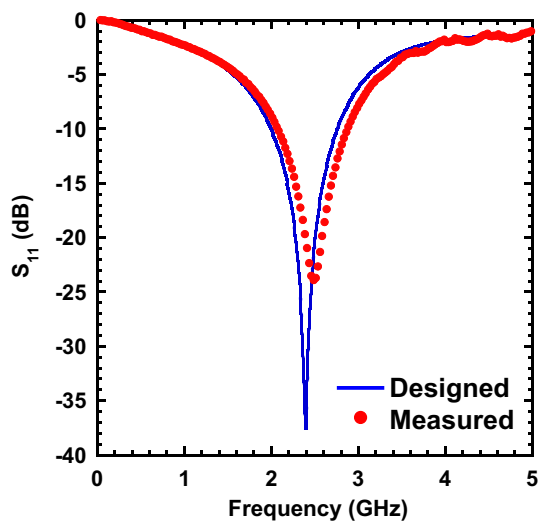
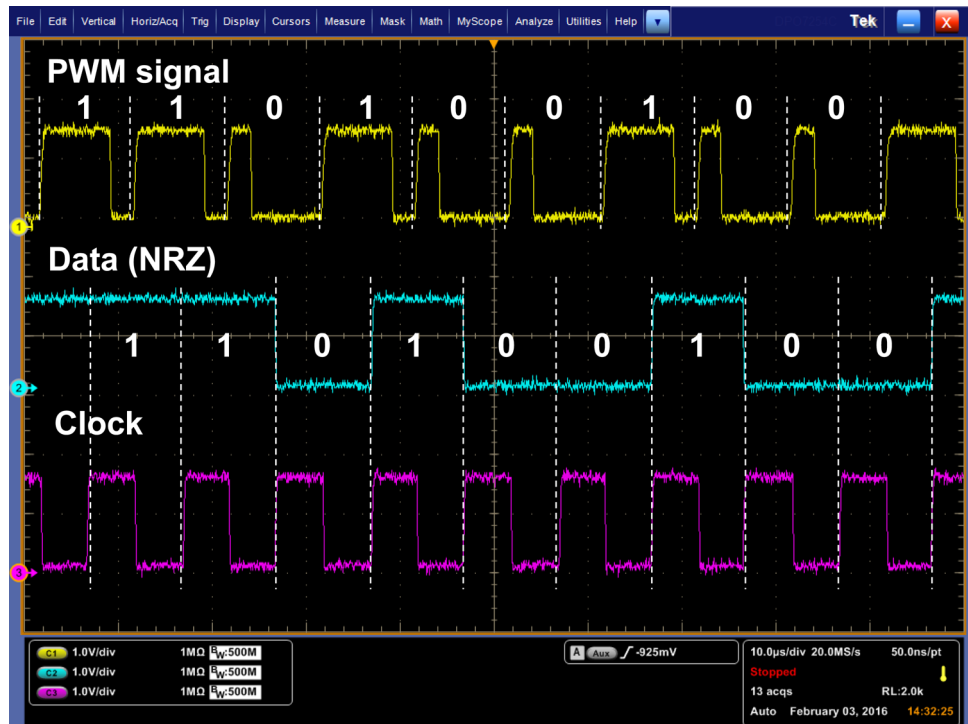


Fig. 9 Return loss S_{11} of WuRx

Figure 9 shows the return loss S_{11} of the WuRx measured with a vector network analyzer. The measured S_{11} matched the designed S_{11} , and good impedance matching of -20 dB was achieved at 2.4 GHz. Figure 10 shows the waveforms of I_{DET} and the square wave applied to the clock output port, where the experimental conditions were

the same as those described in Sect. 2. The substrate noise coupling in the waveform was successfully suppressed when compared with that in the waveform shown in Fig. 4. Table 1 shows the performance comparison among our prototype circuit of this research and related works. In this research, we achieved to integrate and run the WuRx with a CDR, which is a logic circuit, without mixer, LNA and other extra circuits.

5 Conclusion

The substrate noise coupling between the clock recovery circuit and the input port of the envelop detector in a previously fabricated WuRx was investigated experimentally. The propagation path of the substrate noise coupling was clarified by comparing the experimental results with the circuit simulations on the basis of an equivalent circuit model. The design of the WuRx was modified on the basis of the findings to suppress the substrate noise coupling. The fabricated WuRx successfully operated a 100-kbps PWM signal with a carrier frequency of 2.4 GHz, and the effectiveness of the noise coupling suppression recipe was confirmed.

Fig. 10 Waveforms of input port I_{DET} and applied square wave for modified WuRx

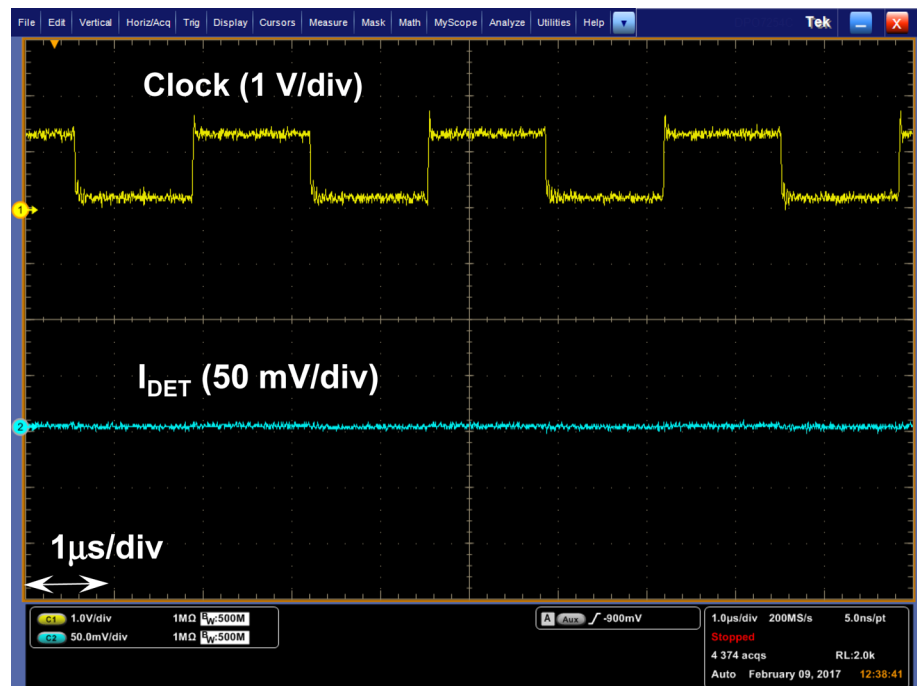


Table 1 Performance comparison of wake-up receivers

References	Power (μ W)	Carrier (GHz)	Sensitivity (dBm)	Bit rate (kbit/s)	Process (nm)	Configuration			
						Mixer	LNA	CDR	External component
[2]	52	2	-72^a	100	90	Yes	No	No	Yes
[3]	51	0.915/2.4	$-75/-64^b$	100	90	No	Yes	No	No
[15]	415	2.4	-82^a	500	65	Yes	No	No	Yes
[16]	2.4	0.868	-71^a	100	130	No	Yes	No	Yes
[4]	6.8	1.75	-47.2^b	1	180	No	No	No	No
[5]	9	60	-68^b	350	180	No	No	Yes	No
[6]	4.5	2.4	-50^a	100	180	No	No	No	Yes
This work	11.3	2.4	$-32^a/-46^b$	100	180	No	No	Yes	No

^aEstimated at a bit error rate (BER) of 10^{-3}

^bEstimated from noise and conversion efficiency

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