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A pipelined SAR ADC with gain-stage based on capacitive charge pump

Kairang Chen[1] · Atila Alvandpour[1]

Abstract This paper presents a 14-bit, tunable bandwidth two-stage pipelined successive approximation analog to digital converter which is suitable for low-power, cost-effective sensor readout circuits. To overcome the high DC gain requirement of operational transconductance amplifier in the gain-stage, the multi-stage capacitive charge pump (CCP) was utilized to achieve the gain-stage instead of using the switch capacitor integrator. The detailed design considerations are given in this work. Thereafter, the 14-bit ADC was designed and fabricated in a low-cost 0.35-µm CMOS process. The prototype ADC achieves a peak SNDR of 75.6 dB at a sampling rate of 20 kS/s and 76.1 dB at 200 kS/s while consuming 7.68 and 96 µW, respectively. The corresponding FoM are 166.7 and 166.3 dB. Since the bandwidth of CCP is tunable, the ADC maintains a SNDR >75 dB upto 260 kHz. The core area occupied by the ADC is 0.589 mm^2.

Keywords Capacitive charge pump · Two-stage pipelined SAR ADC · OTA · Switch capacitor integrator

1 Introduction

Wireless sensor networks are employed in many applications, such as monitoring bio-potential signals, environmental information and interactive multimedia. These applications require high-resolution (>12 bits), low-speed (several kS/s) analog-to-digital converters (ADCs) [1]. Such sensor nodes are usually powered by batteries or energy-harvesting sources [2, 3] hence low power consumption is primary for the constituent ADCs. Normally, tens or hundreds of autonomously powered sensor nodes are utilized to capture and transmit data to the central processor. Hence it is profitable to fabricate the relevant electronics, such as the ADCs, in a low-cost standard CMOS process.

The successive approximation register analog-to-digital converters (SAR ADCs) can provide highly power efficiency solution at moderate resolutions, but achieving a SAR ADC with effective number of bits (ENOB) beyond 12 bits shows enormous challenges due to the influence from comparator noise and capacitor mis-matching [4–6]. The SAR-assisted pipeline ADC is an energy-efficient architecture for high resolution [7]. Such architecture consists of two independent sub-SAR ADCs coupled by a gain-stage. The need of a high-accuracy comparator can be obviated by incorporating a SAR ADC as the sub-ADC in the pipeline stage. However, an additional gain-stage is inevitable to amplify the residue signal. Normally, the switch capacitor (SC) integrator is the primary choice to realize the gain-stage, but a high-gain operational transconductance amplifier (OTA) is necessary to amplify the residue with sufficient accuracy. Since the open-loop DC gain requirement of OTA grows exponentially with the total resolution of the ADC, the design of high-gain OTA is a major challenge for implementing high-resolution pipelined SAR ADC. Meanwhile, as shown in [7–9], the high gain OTA is always a power-hungry block. So, a lower-power alternative way, such as the dynamic amplifier [10, 11], which allows to switch off the OTA during the reset phase but still needs a high open-loop DC gain. In [12], an open-loop amplifier as the gain stage was offered.

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Although the open-loop solution shows a low DC gain, this voltage gain will be deeply influenced by the process variation. So the extra calibration technique is inevitable.

To overcome the high DC gain requirement, in this paper, we employ the design, analysis and implementation of a 14-bit, tunable bandwidth two-stage pipelined SAR ADC in 0.35-µm CMOS process which uses a three-stage capacitive charge pump (CCP) as the gain-stage instead of using SC integrator. Since the basic CCP cell can provide a gain of 2 [13], m-stage CCP can be connected in series to achieve a gain of 2^m. Combining the gain reduction solution as shown in [14], three-stage CCP was utilized to achieve a stage gain of 8. Since the gain reduction solution requires increased sampling capacitance for the second stage sub-ADC to compensate for the reduced signal swing [8], the attenuation DAC [15] was chosen to alleviate the increased capacitance requirement in the second stage. The segmented capacitive array DAC [16] was implemented in the first stage which meets the targeted static linearity with a lower unit capacitance. The prototype ADC achieves a peak SNDR of 75.6 dB at a sampling rate of 20 kS/s and 76.1 dB at a sampling rate of 200 kS/s while consuming 7.68 and 96 µW, respectively.

This paper is organized as follows. Section 2 introduces the proposed pipelined SAR ADC architecture and the operating sequence. Section 3 describes the details of circuit implementation. The measurement results are presented in Sect. 4, followed by the conclusions in Sect. 5.

2 Architecture of the proposed two-stage pipelined SAR ADC

Figure 1 shows the proposed two-stage pipelined SAR ADC architecture. It consists of N_1 bits SAR ADC with segmented binary-weighted capacitive DACs, a multi-stage

CCP and a N_2 bits SAR ADC with split binary-weighted capacitive DACs. For the pipelined SAR ADC, although the resolution of the first stage is N_1, the accuracy for the first stage must meet the total resolution N and also the matching constraints necessitate large unit capacitor in the capacitive array which entails large power consumption and chip area. For the segmented DAC with a segmentation degree k, the unit capacitor value is 2^{k-1} times lower than the unit capacitor for the conventional binary-weighted DAC in order to meet the same targeted static linearity [17]. Hence the SAR ADC with segmented binary-weighted capacitive DAC serves as the first stage in order to relax the unit capacitor value and the active chip area. The multi-stage CCP works as the gain-stage to amplify the residue signal with a inter-stage gain of 2^m where the $m = N_1 - r$ and r is the gain reduction factor [14]. Since the basic CCP cell applies an ideal gain of 2 [13], $N_1 - r$ stages are necessary to achieve a gain of 2^{N_1-r}. The inter-stage gain is reduced by 2^r times, which means an extra capacitor $C_x = (2^{r-1} - 1)C_{tot2}$ is required for the second stage DAC [14] to compensate for the reduced signal swing where the C_{tot2} represents the total capacitance of second DAC. So the SAR ADC with split binary-weight capacitive DAC is chosen to alleviate the increased capacitance requirement in the second stage.

Figure 2 gives the timing diagram of the proposed architecture with three-stage CCP. The input signal V_{in} is sampled through the switch S_1 at the phase f_{s1} marks the beginning of the conversion. The residue signal is generated after $N_1 + 1$ steps conversions. Thereafter, the residue signal is sampled and amplified during phase ϕ_{1_s} and ϕ_{1_a} respectively. The output signal from the first CCP cell will be sampled and amplified by the following stage at phase ϕ_{2_s} and ϕ_{2_a}. So the rest can be done in the same manner until the residue signal is magnified by 8 times.
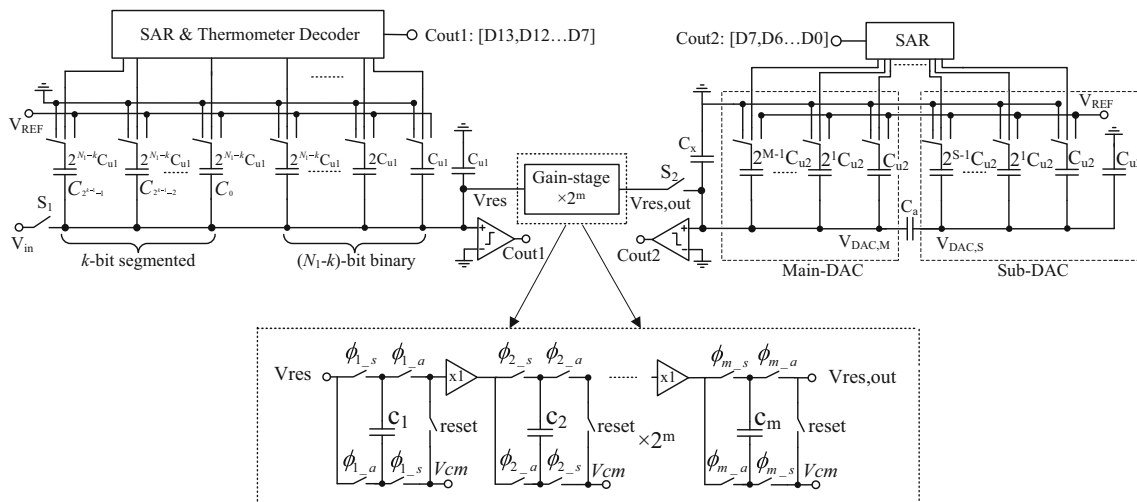

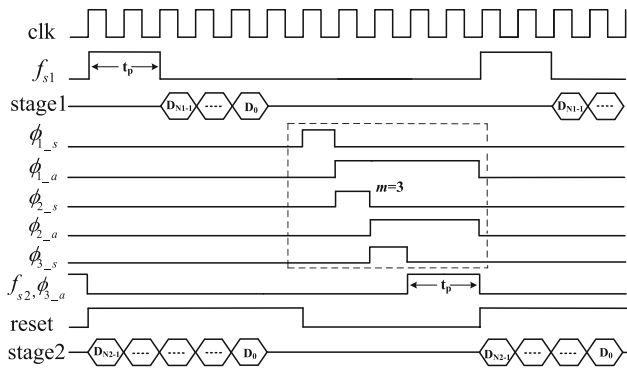Fig. 1 Proposed two-stage pipelined SAR ADC architecture

Fig. 2 Timing diagram for proposed pipelined SAR ADC architecture with $m = 3$

The final output also as the input signal of the second stage will be involved in the following ADC conversion at phase f_{s2} (ϕ_{3_a}). From Fig. 2, the clock frequency can be derived as

$$f_{clk} = (N_1 + 2t_p + m + 1)f_s, \tag{1}$$

where $m = N_1 - r$ is the stage number of gain-stage and t_p is the duration of sampling frequency which is set to $2/f_{clk}$.

3 Proposed pipelined SAR ADC architecture implementation

3.1 Multi-stage CCP analysis and implementation

The multi-stage CCP architecture is shown in Fig. 1, consisting of several basic charge pump cell [13]. For each cell, it supplies a gain of 2. Thus, the multi-stage CCP could achieve a gain of 2^m ideally. In this architecture, the only active circuitry is the unity gain buffer with a capacitive load of C_m. Proper choice of the C_m is crucial for keeping the noise level below the corresponding quantization noise. Meanwhile the choice of the stage number m is also elaborated upon in this section.

3.1.1 Noise analysis

The thermal noise, introduced by the on-resistance of the sampling switch, is the main noise source for the first stage. This noise is sampled by C_1 during ϕ_{1_s} which is given by

$$\overline{v_{n,\phi_{1\_s}}^2} = \frac{kT}{C_1}, \tag{2}$$

where k is the Boltzmann constant and T is the absolute temperature.

For the second stage, the noise is determined by three noise sources which are the noise from the switch in the stage itself, the noise from the previous sampling switch
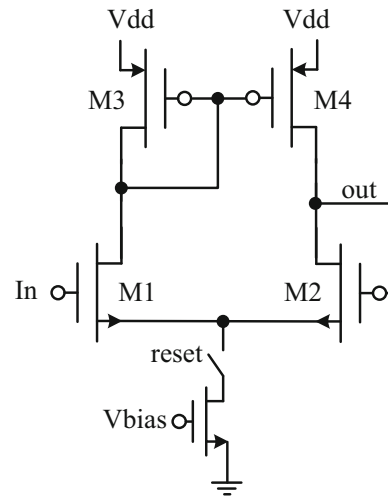
and also the noise from unity gain buffer respectively. The OTA in unity gain configuration as shown in Fig. 3 is employed in this work.

Fig. 3 OTA in unity gain configuration

Because the unit gain frequency of the buffer is $\frac{g_{m1}}{C_2}$, where the g_{m1} is the transconductance of M1 in Fig. 3, the total noise of the resistor is shaped by the low-pass characteristic. So, the total noise power of the resistors is given by

$$\overline{v_{n\_R_{on},\phi_{2\_s}}^2} = \frac{16kTR_{on}}{4\tau}. \tag{3}$$

By using $\tau = \frac{C_2}{g_{m1}}$, where τ is the time constant, the total noise power from resistor is

$$\overline{v_{n\_R_{on},\phi_{2\_s}}^2} = \frac{kT}{C_2}4g_{m1}R_{on}. \tag{4}$$

For the unity gain buffer, the ouput noise power is

$$\overline{v_{n\_OTA,\phi_{1\_a}}^2} = \frac{4kT}{3C_2}\left(1 + \frac{g_{m3}}{g_{m1}}\right), \tag{5}$$

where g_{m3} is the transconductance of M3 in Fig. 3. So, the total noise power sampled by C_2 at phase ϕ_{2_s} is given by the sum of Eqs. (4) and (5) which is

$$\overline{v_{n\_tot,\phi_{2\_s}}^2} = \frac{kT}{C_2}4g_{m1}R_{on} + \frac{4kT}{3C_2}(1 + \frac{g_{m3}}{g_{m1}}), \tag{6}$$

with $g_{m1} = 27.2\,\mu A/V$, $g_{m3} = 10.9\,\mu A/V$, $R_{on} = 8.8\,k\Omega$ and $C_2 = 2\,pF$, the total noise power $\overline{v_{n\_tot,\phi_{2\_s}}^2} = 5.85 \times 10^{-9}$ V^2 at phase ϕ_{2_s}. To verify the noise estimation, the test bench with the first stage was built and simulated in 0.35-µm CMOS process.

Fig. 4 shows the simulation result that is very close to the calculation. Hence the total input referred noise for the first cell is:

$$\overline{v_{n\_tot\_in\_c}^2} = \frac{kT}{C_1} + \frac{1}{(G_s)^2}\left(\frac{kT}{C_2}4g_{m1}R_{on} + \frac{4kT}{3C_2}\left(1 + \frac{g_{m3}}{g_{m1}}\right)\right), \tag{7}$$

where G_s is the stage gain which is 2 ideally for single stage.

The above noise analysis just focus on one single stage. If this single stage is followed by another stage, the noise of the following stage will contribute to the total noise of the previous stage. Equation (6) could stand for the total output noise for each cell. So for the multi-stage charge pump, the total input referred noise can be derived as

$$\overline{v_{n\_tot,input}^2} = \frac{kT}{C_1} + \frac{\overline{v_{n\_tot,\phi_2\_s}^2}}{(G_s)^2} + \frac{\overline{v_{n\_tot,\phi_3\_s}^2}}{(G_s)^4} + \dots + \frac{\overline{v_{n\_tot,\phi_m\_s}^2}}{(G_s)^{2^{m-1}}}. \tag{8}$$

It can be readily seen from (8) that more stages will contribute more noise to the total input referred noise. Thus, a large C_1 is inevitable. For a three-stage CCP, in order to maintain the input referred noise is below the quantization noise of a 14-bit ADC. From (8) and also reusing the parameters from (6), the minimum $C_1 = 2.7$ pF under the assumption that the $C_2 = C_3 = 2$ pF. Meanwhile more stages also indicate more power consumption. Hence, proper choice of stage number is important. Since the gain bandwidth of unity-gain buffer can be changed by tuning the V_{bias} in Fig. 3, the bandwidth of CCP is tunable.

3.1.2 Gain requirement and power analysis

The voltage gain of SC integrator can be shown as

$$G = \frac{1}{\beta}\left(1 - \frac{1}{\beta A}\right), \tag{9}$$

where $\beta = 2^{r-N_1}$ is the feedback factor with the gain reduction factor r and $\Delta e = \frac{1}{\beta A} = \frac{1}{2^{N-N_1}}$ is the gain error caused by the finite open-loop DC gain of the OTA [14]. In order to obtain the same voltage gain by using the CCP architecture, m charge pump stages should be connected in series. The gain of one stage is
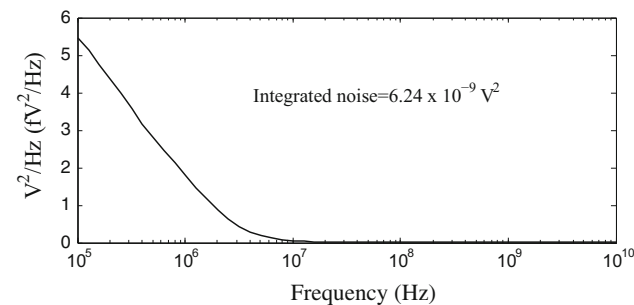

Fig. 4 The total noise in C_2 at phase ϕ_{2_s}

$$G_s = 2G_{buf}, \tag{10}$$

thus

$$(2G_{buf})^m = \frac{1}{\beta}(1 - \Delta e), \tag{11}$$

where the G_{buf} is unity gain of buffer which can be expressed as

$$G_{buf} = 1 - \frac{1}{A_{buf}}. \tag{12}$$

Substituting (12) into (11) and replacing β, Δe with 2^{r-N_1} and 2^{N_1-N} respectively. The DC gain A_{buf} for the OTA in unity gain configuration can be formulated as

$$A_{buf} = \frac{1}{1 - \sqrt[N_1-r]{\left(1 - \frac{1}{2^{N-N_1}}\right)}}. \tag{13}$$

By using $A = 2^{N-r}$ [14] and (13), Fig. 5 plots the DC gain requirement of OTA in SC and CCP for a 14-bit ADC with $N_1 = 7$. It is clear to note that the DC gain for SC grows exponentially whereas it increases linearly for CCP's DC gain. For instance, to achieve a voltage gain with $\Delta e = \frac{1}{2^7}$, the open-loop DC gain of OTA in unity gain configuration is $A_{buf} = 383$ (51.7 dB). However, this DC gain value for OTA in SC integrator is 1024 (60.2 dB). Although the DC gain is reduced, m-stage CCP is needed to achieve a voltage of 2^m. Hence it is worth to analyze the power consumption of CCP.

Following the analysis in [18], the power consumption for a single-stage transconductance amplifier with capacitive feedback is
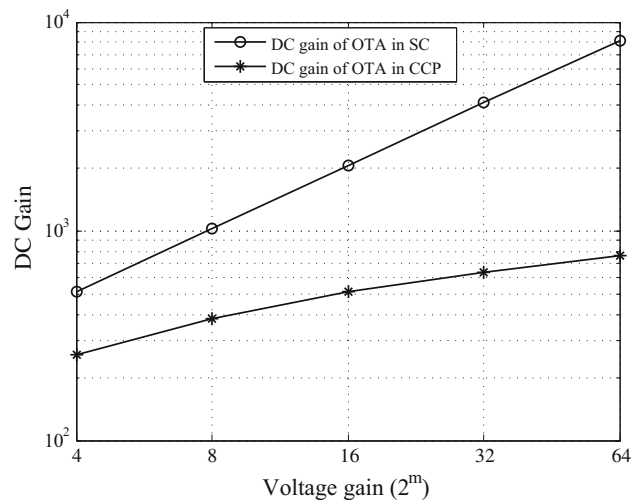

Fig. 5 DC gain requirement of OTA in CCP and SC architecture versus voltage gain (2^m)

$$P_{OTA\_G} = 2V_{FS}^2 f_s C_{LA}\left(1 + (1 + |G|)N\ln 2 \cdot \frac{V_{eff}}{V_{FS}}\right), \qquad (14)$$

where C_{LA} is the capacitive load of OTA, N is total resolution of ADC , V_{FS} is the full-scale range of the ADC and G is the voltage gain. For a MOS transistor in strong inversion, the parameter $V_{eff} = (V_{gs} - V_T)/2$, where V_{gs} and V_T are the gate-to-source and threshold voltages respectively [18]. By replacing G with (9), the (14) can be expressed as

$$P_{OTA\_G} = 2V_{FS}^2 f_s C_{LA}\left(1 + \left(1 + \left|2^m\left(1 - \frac{2^m}{A}\right)\right|\right) \cdot N\ln 2 \cdot \frac{V_{eff}}{V_{FS}}\right).$$
$$(15)$$

For the CCP, the only active circuitry is the unity gain buffer which dominates the total power consumption of CCP. For this OTA, the power consumption is

$$P_{OTA\_1} = 2V_{FS}^2 f_s C_{LA}\left(1 + \left(1 + |1 - \frac{1}{A_{buf}}|\right)N\ln 2 \cdot \frac{V_{eff}}{V_{FS}}\right).$$
$$(16)$$

To achieve a gain of 2^m, m unity gain buffers are needed. To simplify the analysis, we assume that the power consumption of each buffer is equal to the first one's and also ignore the power consumption from switches. Normally, the implementation is fully differential. Hence the total power for m-stage CCP is

$$P_{OTA\_m} = 2m \cdot P_{OTA\_1}. \qquad (17)$$

With $V_{FS} = 3.3$ V, $V_{eff} = 0.3$ V, Fig. 6 plots the OTA energy consumption in CCP and SC architecture according to (15) and (17) as a function of m. To find the influence from larger m, $N = 14$ and $N = 16$ was chosen respectively but with the same load capacitance of 3 pF. In practice, the load capacitance increases along with the growth of resolution. From Fig. 6, the OTA power in SC grows exponentially but linearly in CCP. The CCP consumes more power than SC with lower voltage gain due to more unity gain buffers are used. However, the CCP is more power efficient than SC with high voltage gain which shows a power saving potential for designing higher resolution ADC.

To verify the analysis, the gain-stage utilized the CCP and SC integrator were simulated in 0.35-μm CMOS. In order to find the impacts from the stage number, the voltage gain of 8 and 64 were chosen for the simulation. To achieve the high gain requirement of the OTA in SC integrator, the two-stage OTA with Miller compensation was utilized. During the simulation, half of the sampling period was used as the residue amplification phase. The simulation results show that the DC gain requirement in CCP architecture is 51.8 dB to obtain a voltage gain of 7.94
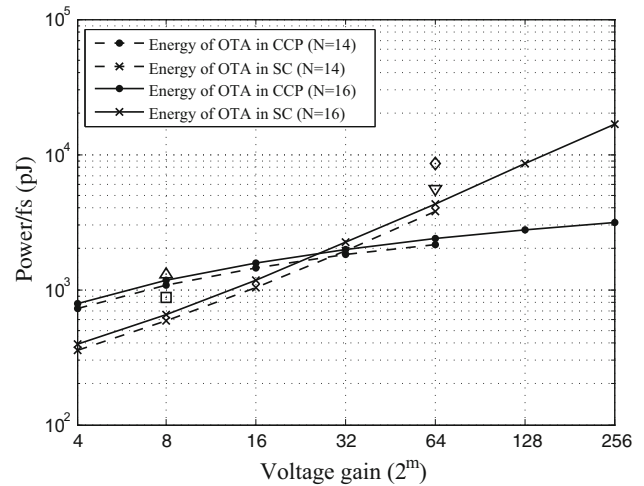

Fig. 6 OTA energy consumption in CCP and SC architecture versus voltage gain (2^m) with $N = 14$, $N_1 = 7$ and $N = 16$, $N_1 = 9$ together with the simulation results (*triangle*: CCP; *square*: SC; *inverted triangle*: CCP; *diamond*: SC)

and the corresponding power is 1.17 μW at 1 kS/s with $C_1 = 3$pF, $C_2 = C_3 = 2$ pF. For the SC integrator, the power is 0.87 μW at 1 kS/s with $C_{LA} = 3$pF but the DC gain is 61.7 dB to achieve the same voltage gain. The CCP's power is higher than SC's due to more unity gain buffers were used. When it comes to the voltage gain of 64, the power of CCP is 5.53 μW at 1 kS/s with $C_1 = 3$pF, $C_2 = C_3 = C_4 = C_5 = C_6 = 2$ pF whereas the power of SC is 8.67 μW with $C_{LA} = 3$ pF at the same sampling rate and the corresponding DC gain requirements are 58 dB for unity gain buffer and 78.5 dB for OTA in SC to get a voltage gain of 63.4. The four simulation results were added into Fig. 6 as well and the above relevant capacitors values are obtained from (8). In Fig. 6, the simulated results are somewhat higher than the predicted results. This is due to the design margin taken into the OTA design.

In this work, the solution of $m = 3$ has been applied to our 14-bit two-stage pipelined SAR ADC project. It should be pointed out that the main purpose of this work was to verify the overall functionality of the proposed multi-stage capacitive charge pump. Compared to the conventional SC integrator, the CCP gain-stage with a voltage gain of 8 is not power-efficient choice for design of a 14-bit ADC. It remains as a future work to find a low-power analog buffer instead of using the unity-gain OTA. However, Fig. 6 suggests that the presented gain-stage would result in higher power efficiency for higher resolutions, for example for 16-bit ADC with 9-bit in the first-stage.

The implementation of unity-gain buffer is shown in Fig. 3 which has a DC gain of 51.8 dB. To determine the impact of process variations and device mismatch on the unity-gain, 200 Monte Carlo simulations were performed. With an external V_{bias} of 0.48 V, Table 1 summarizes the

simulated unity-gain of OTA across process corners, device mismatch and at a temperature range of −40 to 85 °C.

As the table shows the unity-gain OTA shown in Fig. 3 maintains its gain sufficiently constant. To meet the noise requirement of 14-bit ADC, the $C_1 = 3$ pF, $C_2 = C_3 = 2$ pF were chosen. Since the input of gain-stage is discrete time, the normal NMOS transistor was used to achieve the switch. It should be mentioned that one more unity gain buffer is needed between the first stage ADC and the input of gain-stage. The gain error caused by this buffer will be compensated by tuning the reference voltage of second ADC.

3.2 First-stage SAR ADC implementation

For the 14-bit two-stage pipelined SAR ADC, the $N_1 = 7$ was allocated to the first-stage. Aiming to reduce the power consumption and active area of the first-stage, The segmented binary-weighted capacitive DAC was implemented in the first SAR ADC. The reasons are as follows. Since the static linearity of the first-stage is dominated by the capacitor mismatch in the corresponding DAC. Following the detailed analysis in [14], the mismatch-limited unit capacitor for the first-stage with conventional binary-weighted capacitive DAC is

$$C_{u1} > 4.5 K_\sigma^2 K_c 2^{2(N-N_1)}(2^{N_1} - 1), \tag{18}$$

and for the segmented binary-weighted capacitive DAC, the mismatch-limited unit capacitor is

$$C_{u1} > 4.5 K_\sigma^2 K_c 2^{2(N-N_1)}(2^{N_1-k+1} - 1), \tag{19}$$

where K_σ is the mismatch parameter, K_c is the capacitor density and k is the segmented degree. Comparing (18) and (19), it is seen that the C_{u1} for the segmented DAC is 2^{k-1} times lower than that of the conventional DAC. For the poly-insulator-poly (PIP) capacitor in 0.35-μm CMOS process, $K_\sigma = 0.45\%\,\mu m$ and $K_c = 0.86\,fF/\mu m^2$. From (18), the minimum mismatch-limited unit PIP capacitor is 163 fF. However, the segmented DAC requires only $C_{u1} = 40.8$ fF with a segmented degree $k = 3$. Therefore, it will avail power and active area savings by using a segmented

capacitive DAC in the first stage. Here, the minimum mismatch-limited unit capacitance (40.8 fF) is calculated under the assumption that the sampling switch is ideal. In practice, the sampling switch introduces the charge injection and clock feed-through errors which cause additional harmonic distortions. Hence a large unit capacitor of 117.7 fF was required by simulations to achieve the targeted 14-bit ADC performance.

It should be noted that the segmented DAC requires a binary-to-thermometer decoder which lead to extra power consumption and chip area. Larger segmentation degree indicates that the circuit complexity, area occupation and power increase. In [14], the optimal segmentation degree range is $3 \le k \le 5$. In this work, a segmentation degree of $k = 3$ was chosen for the first stage DAC as a trade-off among lower unit capacitor value, increased circuit complexity and power consumption in the digital logic. Figure 7 shows the schematic of the 3-to-7 binary-to-thermometer decoder required for the unary-weighted 3-bit DAC segment which consists of basic logic gates.

Figure 8 shows the control logic circuits which were used to generate the time sequence as shown in Fig. 2. The block diagram of the SAR control logic for the first-stage consisting of two separate shift registers is shown in Fig. 8(a). The upper DFFs chain generate the bit approximation pulses while the DFFs in lower row store the output C_{out} of the comparator. Finally, the switch control signals (D13...D7) for the DAC are generated which will be involved in the ADC conversion. The control logic of the three-stage CCP is illustrated in Fig. 8(b). The first four DFFs are connected in series condition which are used to generate the sampling phase ($\phi_{1\_s}...\phi_{3\_a}$). By choosing the ϕ_{2_s}, ϕ_{3_s} and ϕ_{3_a} as the input of an OR gate, the amplifying phase ϕ_{1_a} can be obtained from the output of OR gate. The ϕ_{2_a} can be implemented through the same way. An AND gate was utilized to create the reset signal by connecting the reverse of four sampling phase. The additional two DFFs with an OR gate are triggered by a "set" signal which subsequently create the sampling signal f_{s1} for

Table 1 Unity-gain OTA performance

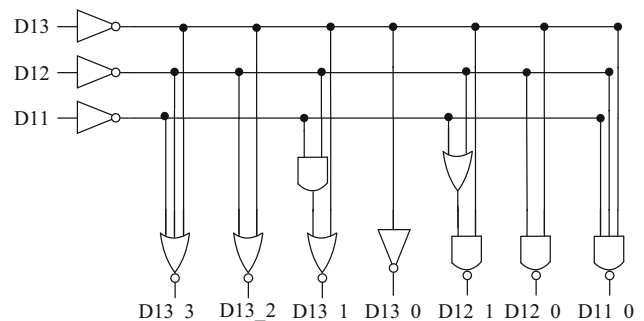| $V_{dd} = 3.3$ V	Unity-gain		
Temperature (°C)	Min.	Max.	3σ
−40	0.9963	0.9978	740.7e−6
0	0.9968	0.9978	563.7e−6
27	0.9968	0.9977	542.1e−6
85	0.9967	0.9977	655.8e−6

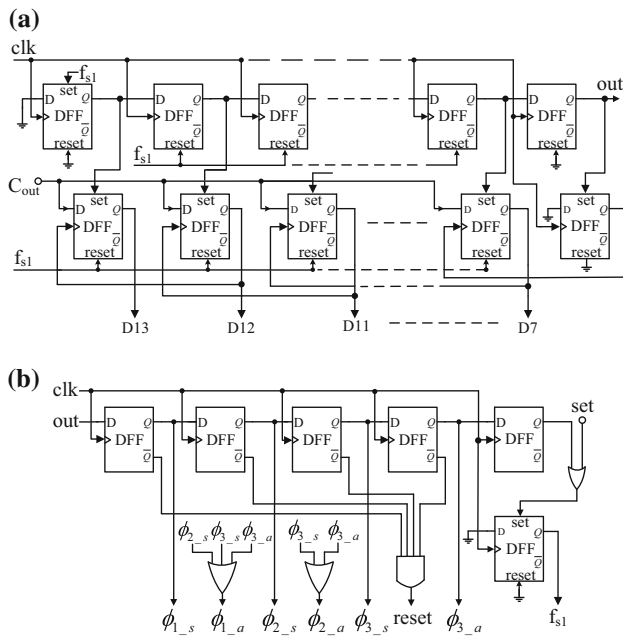**Fig. 7** 3-to-7 binary to unary thermometer decoder

Fig. 8 Control logic. **a** SAR control logic of first stage. **b** Control logic of three-stage CCP

the first-stage and also the f_{s1} as the start signal is connected to the relevant position as shown in Fig. 8(a).

For the input sampling switch S_1 in Fig. 1, the conventional bootstrapped switch [19] is used for improved linearity. Simulation results indicate a linearity corresponding to 17.6-bit for S_1 with a sampling capacitance of 20 pF and 20 kS/s sampling frequency which is sufficient for the 14-bit resolution. The conventional dynamic latch comparator as shown in Fig. 9 is used to generate the digital output bits. Simple inverters have been used to implement the DAC switches.

3.3 Second-stage SAR ADC implementation

A 8-bit SAR ADC with attenuation capacitor based DAC forms the second-stage sub-ADC. The DAC consists of a 4-bit main-DAC and 4-bit sub-DAC. Because of $m = 3$, the extra capacitor $C_x = 112C_{u2}$ was added into the DAC. As the total capacitance of the second sub-ADC (C_{tot2}) is also the load capacitance of the gain-stage, an unit PIP capacitor C_{u2} was chosen as 15.8 fF yielding a $C_{tot2} = 2.0$pF to maintain the total input-referred noise of the gain-stage [Eq. (8)] below the quantization noise of 14-bit ADC. Such choice also satisfies the thermal noise and mismatch requirements of the second-stage ADC's accuracy (11-bit). The SAR logic for the second-stage is similar to that shown in Fig. 8(a) except the reset signal should be connected to ϕ_{3_a} generated by control logic as shown in Fig. 8(b). Since the accuracy of this stage is 11-bit, a transmission gate was used to design the sampling switch S_2 as shown in
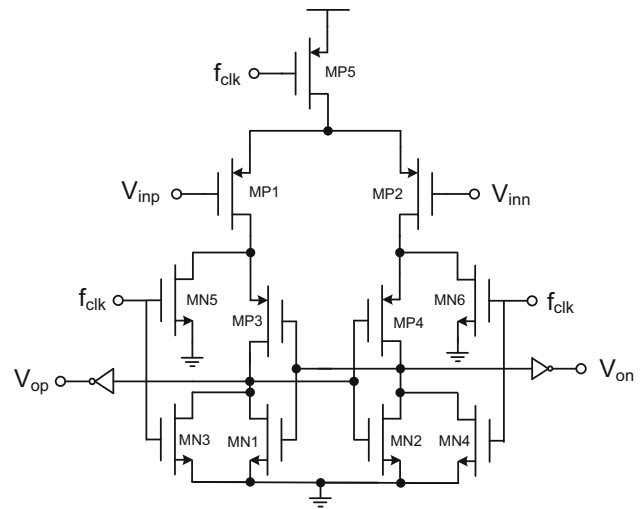

Fig. 9 Dynamic latch comparator

Fig. 1. The same dynamic latch comparator topology as in the first stage is used to generate the digital output bits.

4 Measurement results

The fully differential 14-bit ADC with a core area of $860\mu m \times 685\mu m$ was fabricated in a one-poly-four-metal (1P4M) 0.35-μm CMOS process. The core was packaged in a JLCC44 package. Figure 10 shows the chip micrograph. The unmarked area in Fig.10 includes decoupling capacitors and I/O buffers.

At $V_{bias} = 0.48$ V as shown in Fig. 3, the measured FFT spectrum of the ADC operating at a sampling rate of 20 kS/s with near-DC (0.5127 kHz) and near-Nyquist (9.526 kHz) input tones was shown in Fig. 11. The amplitude of the input signal was set to -0.052 dBFS. A clock frequency of $f_{clk} = 300$ kHz was used. The SNDR, SFDR and ENOB are 75.6, 90.9 dB and 12.27-bit respectively with the near-DC input tone. For the near-Nyquist input tone SNDR, SFDR and ENOB are 74.63, 90.79 dB and 12.1-bit respectively.

By increasing the V_{bias} to 0.63 V, the ADC can work at a sampling frequency of 200 kHz. Fig. 12 shows the measured FFT spectrum with near-DC and near-Nyquist input tones but under a sampling rate of 200 kS/s. With the same amplitude of the input signal, the measured SNDR is 76.11 dB, providing a 12.35-bit ENOB with near-DC input. For the near-Nyquist input, the ADC also achieves a 74.47 dB SNDR and 12.08-bit ENOB. The SNDR and SFDR over the range of input signal frequencies upto the Nyquist bandwidth for 20, 200 kS/s are shown in Fig. 13. The SNDR >74 dB is maintained upto the Nyquist bandwidth for the two sampling rates.
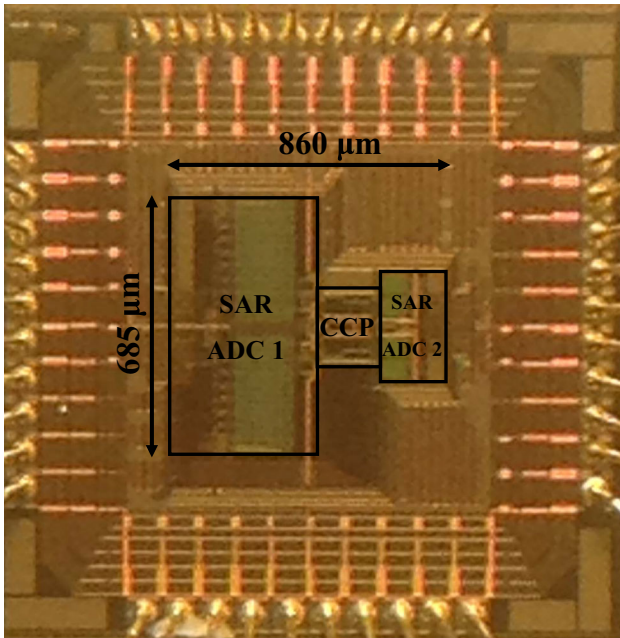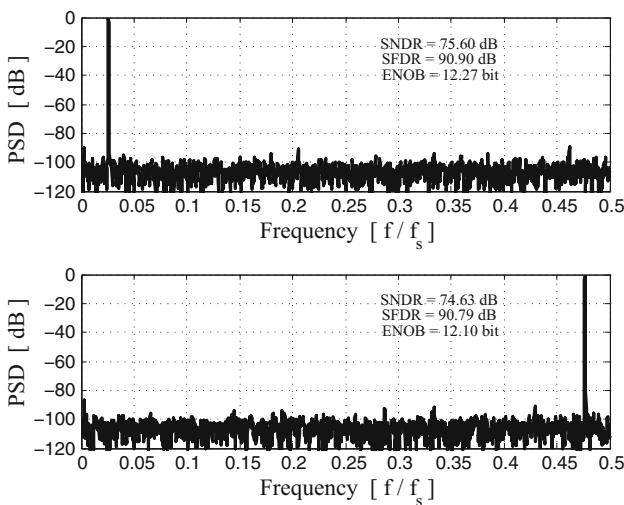
Fig. 10 Die micrograph

Fig. 11 Measured 4096-point FFT spectrums with near-DC ($f_{in} = \frac{105}{4096}f_s$) and near-Nyquist ($f_{in} = \frac{1951}{4096}f_s$) inputs at 20 kS/s

Since the bandwidth of CCP is tunable, Fig. 14 shows the measured SNDR versus the sampling rate under the different V_{bias} setting. By increasing the bandwidth of CCP, the proposed ADC achieves a SNDR >75 dB upto 260 kS/s. Due to the speed limitation of comparator and sampling switch, the ADC performance drops fast after f_s = 260 kHz.

Histogram test was used to measure the static linearity of the ADC. A full swing, differential sinusoidal input tones (f_{in} = 14.64 Hz at f_s = 20 kHz, f_{in} = 146.48 Hz at f_s = 200 kHz) were applied to the ADC. The measured differential nonlinearity (DNL) and integral nonlinearity (INL) for 20 and 200 kS/s are shown in Figs. 15 and 16.
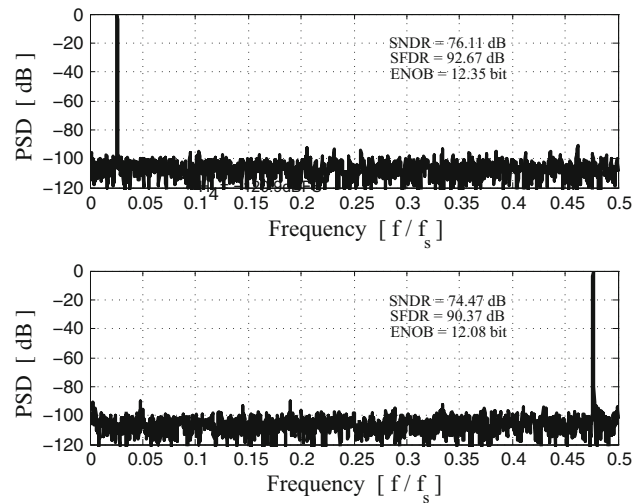

Fig. 12 Measured 4096-point FFT spectrums with near-DC ($f_{in} = \frac{105}{4096}f_s$) and near-Nyquist ($f_{in} = \frac{1951}{4096}f_s$) inputs at 200 kS/s
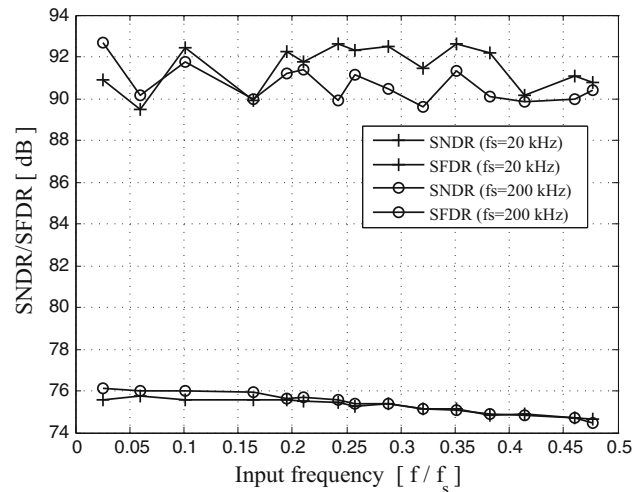

Fig. 13 Measured SNDR and SFDR at 20 kS/s (V_{bias} = 0.48 V), 200 kS/s (V_{bias} = 0.63 V) versus input frequency
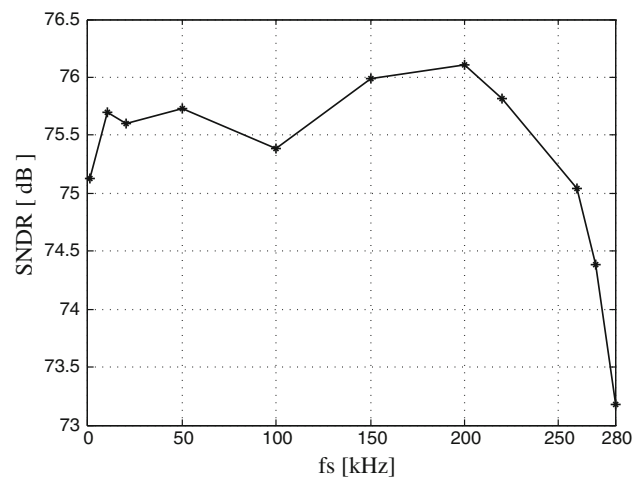

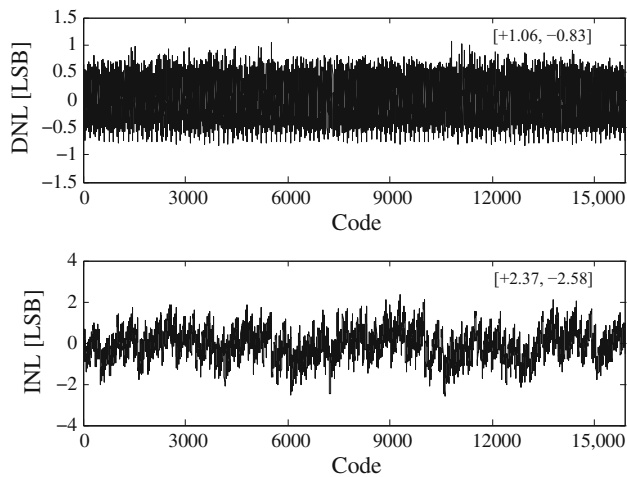**Fig. 14** Measured SNDR versus fs with near-DC input ($f_{in} = \frac{105}{4096}f_s$)
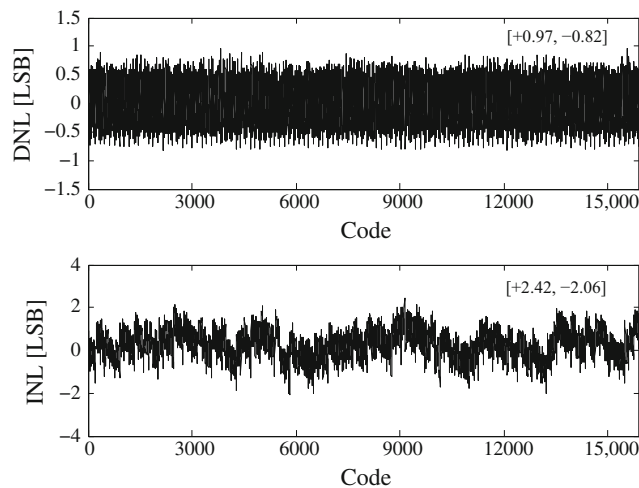
Fig. 15 Measured DNL and INL at 20 kS/s

Fig. 16 Measured DNL and INL at 200 kS/s

The peak DNL and INL are 1.06/−0.83 LSB and 2.37/−2.58 LSB for 20 kS/s. For the 200 kS/s sampling rate, the peak DNL and INL are 0.97/−0.82 LSB and 2.42/−2.06 LSB, respectively.

With a supply voltage 3.3 V for analog and 3 V for the digital, the total power consumption of the ADC is 7.68 μW at f_s = 20 kS/s and 96 μW at f_s = 200 kS/s. For 20 kS/s sampling rate, about 40.6 % of total power was consumed by the digital, 26.9 % by the CCP, 20 % by the DAC and 12.5 % by the comparator. For 200 kS/s, the corresponding percentages are 32.7, 41.8, 15.5 % and 10 %, respectively. Due to the increased V_{bias}, the CCP occupies more power with sampling rate of 200 kS/s. Table 2 compares the performance of proposed ADC with other high-resolution pipelined SAR, pipelined and nyquist ADC. The Schreier FoM defined by

$$\text{FoM} = \text{SNDR} + 10\log\left(\frac{\text{BW}}{\text{P}}\right) \tag{20}$$

has been used to compare the performance of the ADCs. The proposed ADC achieves a peak FoM of 166.7 dB at 20 kS/s and 166.3 dB at 200 kS/s. Compared to the implementations in 0.35-μm CMOS reported in [20, 21, 22] this work achieves a best FoM. The achieved FoM is also comparable to the reported result from [8]. Hence, the proposed solution offers an attractive choice for designing the high resolution pipelined SAR ADC without designing a high DC gain OTA.

5 Conclusion

The three-stage capacitive charge pump as the gain-stage for a 14-bit two-stage pipelined SAR ADC was presented in this work. Due to the tunable bandwidth of CCP, The proposed ADC achieves a SNDR >75 dB upto 260 kHz. Meanwhile the ADC also provides a competitive FoM among related works. By employing the CCP as the gain-

Table 2 Comparison of the ADC with other high-resolution ADCs

	[20]	[21]	[22]	[8]	[9]	[11]	[23]	This work	
CMOS (nm)	350	350	350	130	65	28	65	350	
Architecture	Pipelined with SC	Pipelined withSC	Pipelined withSC	SAR-assisted withSC	SAR-assisted with Ring amplifier	SAR-assisted with DynamicSC	Nyquist SAR	SAR-assisted with CCP	
Resolution (bit)	14	14	12	14	13	14	14	14	
Calibration	N0	No	Yes	No	No	Yes	No	No	
DC gain	100 dB	–	60 dB	86 dB	>80 dB	–	–	51.8 dB	
Area (mm²)	7.8	–	20.6	0.24	0.054	0.137	0.28	0.589	
fs	75 MS/s	80 MS/s	20 MS/s	30 MS/s	50 MS/s	80 Ms/s	10 kS/s	20 kS/s	200 kS/s
SNDR (dB)	74	74	72.5	70.8	71.5	68.0	78.1	75.6	76.1
SFDR (dB)	94	100	84.4	87.8	87.0	80.7	88.5	90.9	92.7
Power	318 mW	1200 mW	56.3 mW	2.54 mW	1.0 mW	1.5 mW	2.48 μW	7.68 μW	96 μW
FoM (dB)	154.7	149.2	155	168.5	175.5	172.3	171.1	166.7	166.3

stage, the high DC gain OTA in the SC integrator was avoided while also reducing the design complexity. So, we concluded that the multi-stage capacitive charge pump shows an another solution to achieve the function of the gain stage instead of using the SC integrator for the low-speed, two-stage pipelined SAR ADC application.

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