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Analysis and design of wideband distributed VCOs based on switched-cells tuning technique

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Abstract The paper discusses a VCO belonging to the class of Distributed-VCOs (DVCOs) designed for wide tuning range operations. The trade-off between wide bandwidth and phase noise is central to the proposed design and the paper covers the DVCO topology and discusses its operations in detail, starting by the general conditions of oscillation and covering the applied tuning techniques. In particular the paper reports a description of the so called "switched-cells tuning technique". The design of a fully integrated DVCO is reported. It is based on the "switched-cells tuning technique" and provides the following measured tuning ranges over four sub-bands: 219 MHz around 900, 291 MHz around 1.5 GHz, 392 MHz around 1.8 GHz and 199 MHz around 2.4 GHz. The DVCO performances are discussed and compared with other similar implementation reported in the recent literature showing the potentialities of the proposed approach. According to the reported theory, the results show the applicability of the proposed Distributed VCOs for wide bandwidth applications.

Keywords Voltage-controlled oscillators · Microwave circuits · Switched circuits · Distributed amplifier

1 Introduction

Multi-band, multi-standard requirements dominate modern wireless telecommunications most of all in advanced systems based on the paradigm of Software Defined Radios (SDR) [1] both at the lower GHz and higher GHz bands [2, 3]. In these implementations the VCO design faces a difficult trade-off between wide tuning range and phase noise.

Different techniques are possible to design a wideband VCO: transformer based VCOs [3], frequency translation (division, multiplication, injection locking) [4], multiple VCOs [5], switched inductors based VCOs [6], multiple inductors based VCOs [7], inductor reuse based VCOs [8]. These tuning techniques are commonly adopted at low frequencies and there is a great interest in adopting similar approaches at higher frequencies.

DVCOs have been introduced to obtain a wide tuning range while providing good phase noise as an alternative to ring oscillators, which usually provide wide tuning range and poor phase noise, and LC-VCOs, which provide better phase noise over smaller bands. A DVCO is based on a Distributed Amplifier (DA) operating in the reverse gain mode [9–12], or in the forward gain mode [13–20]. DVCOs are also known as travelling wave VCOs which belong to the class of wave-based oscillators wherein there are the rotary-travelling wave VCOs (also called closed-loop Distributed VCOs) and standing-wave VCOs [21].

Theoretically, the DVCO could benefit of the wide bandwidth of the amplifier and, avoiding passive components, it allows to design fully integrated VCOs which operate at higher frequencies when compared to the integrated LC-VCOs for a given technology. The literature proposes several examples of DVCOs operating in the forward gain mode [13–20], but none of these solutions exploits completely the potentiality of such class of oscillators in terms of wide tuning range.

The topologies proposed in [22] and [23] aim to take advantage of the wide bandwidth of the DA to design a wide tuning range VCO. The approach proposed in [23], is based on the idea to separate the amplification from the

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phase shifting. In this way the DA can play the role of a "loop-gain tank". Therefore, the amplifier potentially provides the oscillation sustainment over a very wide bandwidth while giving an uniform phase noise, output power and harmonics suppression. A key aspect of this topology is how the phase shifting is implemented to exploit the DA potentialities.

Section 2 discusses the operation of this type of DVCO and the general condition of oscillations. Section 3 introduces a study on the implementation of the phase shifting techniques for wideband applications. To validate the proposed "switched cell tuning technique" a fully integrated DVCO prototype operating at low GHz has been implemented and its performances are reported in Sect. 4. The potentialities of the proposed approach are evidenced in this section comparing the prototype measurements with the literature.

2 Distributed VCO

In the classical DVCO the DA amplifies and simultaneously assures the right phase shift between the gate (base) and the drain (collector) transmission lines, so that the Barkahusen criteria is satisfied. Assuming equal propagation properties for both transmission lines into the DA, the oscillation frequency, f_o, is [13]:

$$f_o \approx \frac{v_{phase}}{2nl} \approx \frac{1/\sqrt{LC}}{2nl} = \frac{\pi f_c}{2nl} \quad (1)$$

where v_{phase} is the phase velocity along the transmission lines, l is the length of the single cell, n is the number of transistors, L and C are the inductance and the capacitance per unit length and f_C is the cut-off frequency of the loaded transmission lines. According to (1), there are two possibilities for achieving the tuning: to change the phase velocity and/or the effective length of the transmission lines.

In practical implementations, the number of transistors is limited by the losses in the DA, and it does not exceed 3–4. Therefore, the DA operates at a frequency close to f_C introducing some drawbacks: the characteristic impedance of transmission lines strongly varies with the frequency; the attenuation of the transmission lines, due to impedance mismatches, increases and the noise figure of the DA increases as well.

To overcome these limits, the basic idea is to split the DVCO into two blocks: the DA followed by a Synthetic Line (SL) (Fig. 1) [23]. This allows to design a DVCO with a wide tuning range while providing small variations of the output power, reduced phase noise and low harmonic generation over the entire band [24].

In this topology, the DA must introduce enough inverting gain to sustain the oscillation over a wide bandwidth, according to its distributed nature, regardless of the required phase shift. Therefore, the transmissions line cut-off frequency in the amplifier, $f_{C,amp}$, can be set far enough from the tuning band upper limit.

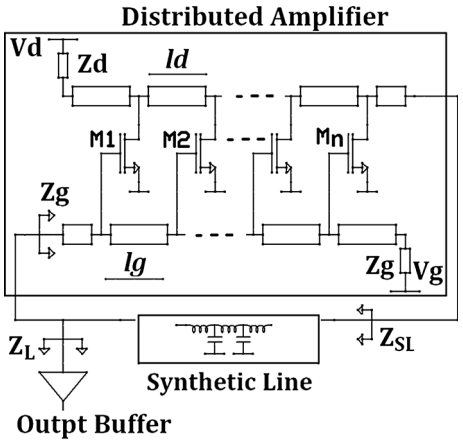

Fig. 1 DVCO topology

The phase shift required for the oscillation is controlled by the SL which is, in its basic version, an m-cells periodic structure. The electrical behavior of the SL depends on the topology of its basic cell.

The tuning obtained by varying the electrical parameters of the SL does not affect the in phase power-sum at each tap point on the drain (collector) line of the DA, allowing a greater frequency variation without the switching off of the oscillation. An additional degree of freedom is given by the choice of the SL cell topology, depending on the circuit requirements.

The advantage of this approach, first of all, is that the characteristic impedance, Z_0, of the DA is almost constant all over the tuning band. At the same time, a flat behavior is ensured over the entire tuning band by the DA itself along with an optimum noise figure at its center band which translates in better phase noise performances. The uniformity of the performances in terms of output power, phase noise and harmonics suppression all over the wide tuning range, achievable by using this topology is very important for wide bandwidth VCOs.

Similar techniques, based on the use of two blocks, govern the operations of other oscillators for achieving a wide tuning range. Some examples are those based on uniform or multi-section transmission lines described in [25] and the ring oscillator presented in [26] where the LC delay lines are used to reduce the errors in the free-running frequency caused by process variations.

2.1 The general condition of oscillation

It is possible to obtain the general conditions of oscillation generalizing the equation derived in [13]. To this purpose,

it is useful to calculate the open loop gain given by the product of the individual gain in the cascade of the DA and the SL as shown in Fig. 2. The DA contains n transistors and two transmission lines. In the following we assume a MOS implementation but similar consideration can be made for the bipolar case. The forward wave on the gate line is amplified by the transistors and absorbed by the termination matched to characteristics impedance of the gate line, Z_g. If the incident wave on the drain line travels with the same phase velocity, then each gain stage adds power in phase to the signal at each tap point on the drain line, the backward wave on the drain line is absorbed by the termination matched to characteristics impedance of the drain line, Z_d. Assuming that the spacing between the transistors is smaller than half wavelength then their input and output impedances can be considered distributed and added to the parameters per unit length of the transmission lines.

The DA gain can be calculated from the circuit reported in Fig. 3.

The impedance, Z_k, seen at kth tap of the drain line is $Z_d//Z_{SLK}$, where Z_d is the characteristics impedance of the drain line and Z_{SLK} is the input impedance of the SL transformed along the path to the kth tap point along the drain transmission line:

$$Z_k = \frac{Z_d}{2}\left(1 + \Gamma_{SL} \cdot e^{-\gamma_d (n-k+1) l_d}\right) = \frac{Z_d}{2}(1 + \Gamma_{SL}^k) \tag{2}$$

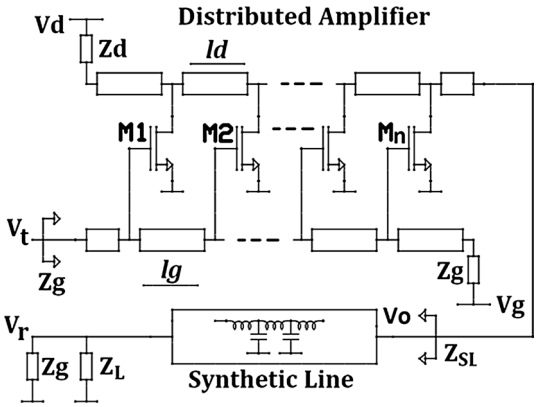

Fig. 2 DVCO open loop

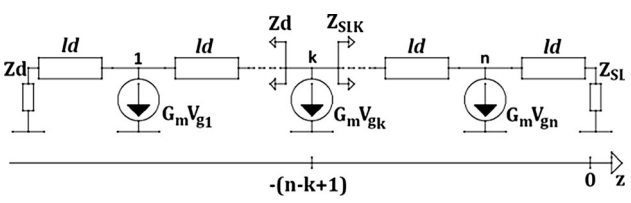

Fig. 3 Equivalent circuit of the drain line

where Γ_{SL} is the reflection coefficient at the input of the SL and γ_d is the complex propagation constant of the loaded drain line. The voltage at the k_{th} tap point is:

$$v_{dk} = -\frac{G_m Z_d}{2}(1 + \Gamma_{SL}^k) v_{gk} \tag{3}$$

where G_m is the large-signal transconductance of each transistor. The voltage at the k_{th} tap point of the gate line is related to the gate line segment l_g and to the complex propagation constant of the loaded gate line γ_g:

$$v_{gk} = v_{in} \cdot e^{-\gamma_g k l_g} \tag{4}$$

where v_{in} is the voltage at the input node of the DA. The voltage, v_o, across the load Z_{SL} can be determined by using the superposition method. The contribute to v_o due to the k_{th} transistor is:

$$v_o^k = \frac{(1 + \Gamma_{SL}) \cdot e^{-\gamma_d (n-k+1) l_d}}{(1 + \Gamma_{SL}^k)} v_{dk} \tag{5}$$

By substituting in (5), (3) and (4), it is possible to achieve the following expression:

$$v_o^k = -\frac{G_m Z_d}{2}(1 + \Gamma_{SL}) \cdot e^{-\gamma_d (n-k+1) l_d} \cdot e^{-\gamma_g k l_g} v_{in} \tag{6}$$

Summing all the contributions, v_o is expressed by:

$$v_o = -\frac{G_m Z_d}{2}(1 + \Gamma_{SL}) v_{in} \sum_{k=1}^{n} e^{-\gamma_d (n-k+1) l_d} e^{-\gamma_g k l_g} \tag{7}$$

Using the identity, $a_n - b_n = (a-b)(a_{n-1} + a_{n-2b} + \cdots + b_{n-1})$, the previous equation becomes:

$$v_o = -\frac{G_m Z_d}{2}(1 + \Gamma_{SL}) v_{in} e^{-(\gamma_d l_d + \gamma_g k l_g)} \frac{e^{-\gamma_d n l_d} + e^{-\gamma_g n l_g}}{e^{-\gamma_d l_d} + e^{-\gamma_g l_g}} \tag{8}$$

Finally, the DA gain is expressed by:

$$A_{DA} = -\frac{G_m Z_d}{2}(1 + \Gamma_{SL}) e^{-(\gamma_d l_d + \gamma_g k l_g)} \frac{e^{-\gamma_d n l_d} + e^{-\gamma_g n l_g}}{e^{-\gamma_d l_d} + e^{-\gamma_g l_g}} \tag{9}$$

In the case of $\gamma_g l_g = \gamma_d l_d = \gamma l$, the voltage gain is equal to:

$$A_{DA} = -n\frac{G_m Z_d}{2}(1 + \Gamma_{SL}) e^{-\gamma (n+1) l} \tag{10}$$

In the previous equations it has been considered the case of a matched load, Z_d, connected to the drain line which absorbs the reflected wave. By using the previous approach, it is easy to generalize the expression of the DA gain when a generic load impedance is connected to the drain line.

The gain of the second stage is the ratio between the voltage, v_o, calculated before, and v_r (Fig. 2). The SL is a cascade of m identical cells, and can be modeled as a transmission line. By using the relation between the values

of voltages along a transmission line, it is possible to express as follows the gain of the second stage:

$$A_{SL} = \frac{(1+\Gamma_L)\cdot e^{-m\gamma_{sl}}}{(1+\Gamma_L\cdot e^{-2m\gamma_{sl}})} = \frac{(1+\Gamma_L)\cdot e^{-m\gamma_{sl}}}{(1+\Gamma_L^m)} \tag{11}$$

where Γ_L is the reflection coefficient at the output section of the SL while γ_{sl} is the complex propagation constant of the SL; the expression of γ_{sl} depends on the type of cell into the SL.

The open loop gain is equal to $A_{DA} \times A_{SL}$. In the case of $\gamma_g l_g = \gamma_d l_d = \gamma l$, the open loop gain is:

$$A_{ol} = -n\frac{G_m Z_d}{2}(1+\Gamma_{SL})e^{-\gamma(n+1)l}\cdot\frac{(1+\Gamma_L)\cdot e^{-m\gamma_{sl}}}{(1+\Gamma_L^m)} \tag{12}$$

Finally the general conditions of oscillation is expressed by the following equation:

$$\frac{(1+\Gamma_L)\cdot e^{-m\gamma_{sl}}}{(1+\Gamma_L^m)}\cdot\frac{G_m Z_d}{2}(1+\Gamma_{SL})e^{-(\gamma_d l_d+\gamma_g k l_g)} \times \frac{e^{-\gamma_d n l_d}+e^{-\gamma_g n l_g}}{e^{-\gamma_d l_d}+e^{-\gamma_g l_g}} = -1 \tag{13}$$

This expression sets both the amplitude and the frequency of oscillation. In the case of $\gamma_g l_g = \gamma_d l_d = \gamma l$, the previous equation becomes:

$$\frac{(1+\Gamma_L)\cdot e^{-m\gamma_{sl}}}{(1+\Gamma_L^m)}\cdot n\frac{G_m Z_d}{2}(1+\Gamma_{SL})e^{-\gamma(n+1)l} = -1 \tag{14}$$

3 The tuning techniques

The most common techniques used for the classical DVCO operations are inherent-varactor and delay-balanced current steering tuning [13]. Other techniques are the delay variation by positive feedback tuning technique [15] and the current starving method [20]. The inherent-varactor tuning allows to vary the oscillating frequency by modifying the phase velocities along the gate (base) and drain (collector) lines in the DA. This change is achieved by controlling the DC bias voltage of the active components of the DA which in turn varies the capacitances along the lines, thus inducing the desired phase-shift variation. This solution is well suited for integration, because it does not require external components. On the other hand, the variations induced in the transistors bias point are unacceptable when a wide tuning range is required, because they usually bring to the damping of the oscillation. Moreover, the capacitances in the two SLs do not vary with the same rate when the DC voltage varies, thus, generating a difference in phase velocity which does not allow the in-phase sum of the contributions along the gain line. This condition results in strong amplitude variations of the oscillation in the tuning band.

The delay-balanced current steering tuning technique varies the effective basic cell line length using the current-steering technique. Usually this solution is used to finely tune the oscillation as it offers less tuning span than the inherent-varactor technique.

As previously discussed, in the DVCO based on the splitting in two blocks: the DA followed by a SL, the DA acts as a "loop-gain tank" and has the capability to sustain the oscillation over a wide bandwidth. Given a set of specs for the oscillator, the SL has to be designed in order to take advantage of the DA operations. The weak interaction between the tuning controlled by the SL and the gain inserted by the DA gives the possibility to implement new tuning schemes.

A possible arrangement for the SL is described in [27] using switched-capacitors banks. These are commonly used in LC-VCOs design to achieve a coarse variation of the capacitance, C, which governs the oscillation frequency. This variation, ΔC, is usually controlled by exploiting a digital tuning scheme.

A second solution to design the SL is based on the use of the "switched-cells tuning technique" proposed in [28] which seems to be a suitable way to implement a SL that guarantees wideband operations.

These two tuning techniques add to the basic topology described in [23] and [24] the multi-band capability, extending in this way the potentialities of this kind of DVCO. Comparing these two solutions, the technique introduced in [28] and used in this work, seems to be the better way for fully exploiting the wideband DA. In fact the switched-cell tuning technique allows a weaker interaction between the SL and the DA than the switched-capacitors banks technique. Moreover the use of the switched bank of varactors, described in Sect. 4, allows to overcome some limits of the DVCO reported in [28] making this topology suitable for practical implementations of wideband DVCO.

3.1 The switched-cells tuning technique

The frequency of oscillation depends on the length of the path that the signal has to undergo inside the loop, the longer is the path the lower is the frequency that fulfills the Barkhausen criterion. The key point is to implement a suitable tuning technique that is able to modify the path without leading to the switching off of the oscillation. In order to achieve this result, the change should not introduce a significant variation into the operation of the DVCO both in the first and in the second block. In particular, the impedance changes when the phase velocity along the SL varies performing the tuning in each sub-band. Such tuning, thus, must be as insensitive as possible to the load impedance variations presented at the input port of the SL

to the DA in order to not modify the operation of the DA itself. The "switched-cells tuning technique" is able to meet this requirement. Moreover the loss in the SL should remain constant after the change in the length of the path. Actually, this is harder to achieve due to the fact that the losses increase inherently extending the path. Operating only on the SL it is not possible to solve this problem and then it is necessary to take into account the increased losses and compensate them with the gain of the DA.

The "switched-cells tuning technique" introduced in [28] is based on the simple idea of modifying the number of cells in the signal path into the SL by using a digital control scheme to implement the coarse jumps among the sub-bands of the multi-band DVCO. The periodic m-cells structure introduces approximately a phase shift, equal to m times the unitary phase shift, $\varphi_{sc,}$ the higher is the number of cells the more this approximation is correct. In practical implementations the loading that each cells has at its ports need to be properly taken into account [29]. Assuming the use of the same DA with three different periodic structures using the same basic cell but with different cell numbers m_1, m_2, m_3 with $m_1 < m_2 < m_3$, since the oscillation frequency is determined by the phase shift equal to 360° along the loop, the corresponding three DVCOs oscillate at different frequencies respecting the following relation: $f_{osc1} > f_{osc2} > f_{osc2}$.

Two implementations are possible (Fig. 4). In the first one, the necessary phase shift is introduced by choosing the right branch (Fig. 4(a)). In the second one, the blocks are arranged in a cascaded structure (Fig. 4(b)). The number of different paths corresponds to the number of multi-bands of synthesis. In both the configurations depicted in Fig. 4, there are three available different lengths of the signal path.

An important difference between these two configurations is the fact that in the parallel topology the cells number in each branch is equal to the number of cells necessary for the wanted band of synthesis associated with such branch. In the cascade topology the number of cells inserted into the path is the sum of the number of cells inside the blocks activated by the SPDTs. For a given design adopting the same cell topology, the parallel configuration has a higher number of cells than the cascade one. It represents a disadvantage in the case of an integrated implementation of the proposed topology in terms of area used on chip by the second block. On the other hand in the cascade topology the loading made by each block on the others is a design key point. In the parallel topology the matching is considerably relaxed because each branch is inserted in the loop separately. In both the solutions an important key point is to take into account the role of the parasitic introduced by the switches. Let N be the number of desired sub-bands, in the parallel architecture the main problem introduced by the switches are the N-1 parasitic off-capacitances which represent a not negligible load at

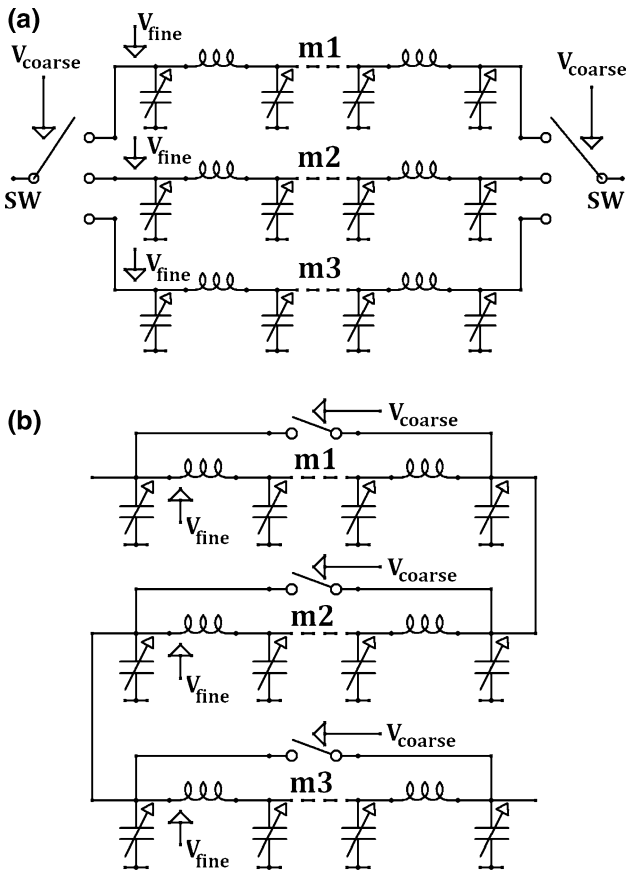

Fig. 4 Two possible simplified implementations for the switched-cell structure: **a** parallel and **b** cascaded approach

the edges of the synthetic line. With a π-cell topology it is easier to absorb these parasitic into the parameters of the line. For the cascade architecture the parasitic capacitive loading is smaller and the main problem are the increased and variable losses introduced by the switches depending on the number of switches in the "on state".

Therefore the cascade architecture is the better solution primarily in terms of area consumption, while the parallel topology simplifies the matching design. The fine tuning inside each sub-band is made by varying the phase velocity along the inserted cells into the loop using the varactors in each cell.

3.2 Some considerations on the design

The choice of the single cell topology and the bias point are the main key aspects affecting the DVCO performances.

3.2.1 Single cell topology

The SL mentioned so far, refers to the second block of the DVCO. Actually also the two transmission lines of the DA can be implemented as SLs. Specially in this case, the

choice of the better topology of the elementary cell in an RFIC implementations becomes an important design point. The simpler topologies are the T cell and π-cell. Considering the electrical equivalent model of an integrated inductor, the π-cell allows to have simultaneously two advantages: to reduce the number of inductors and to facilitate the matching. While the first advantage is an intrinsic feature of this topology, the second advantage comes from the electrical equivalent model of an integrated inductor. Indeed, it is a π-cell, then, the parasitic elements can be absorbed completely into the basic cell components that constituted the SL, in the same way used to absorb the input and output impedances of the transistors. Differently, in the case of T-cell, the parasitic capacitances at the edges of the SL cannot be absorbed. For these reasons it is possible, by using π-cells, to obtain more predictable transmission lines.

3.2.2 Bias point in the DA

Another design issue is the choice of the best bias point that reduces the harmonics of the generated signal inside the DA. Unlike classical DVCO, there is not filtering inside the DA itself, the filtering which reduces the harmonics is introduced by the SL. Although the output of the DVCO is a clean waveform, it is important to choose a proper bias point in order to stabilize the oscillation. The phase shift introduced by the SL is set by modifying the value of the phase velocity along this line. This change varies the cutoff frequency, f_{cSL}, of the line as well. Then, there is a direct relation between the filtering performed by the SL and the phase shift needed for the oscillation. The greater is the phase shift introduced by the SL, the smaller is the cutoff frequency and the higher is the filtering. For this reason the filtering is theoretical slightly more effective for frequencies of oscillation near the lower edge of the range of synthesis.

4 Measurements and results

The fully integrated DVCO has been designed and tested using a low-cost 0.35 μm SiGe technology. The prototype comprises the DA, the SL, the output buffer and a decoder used for managing the coarse tuning. The size of the final layout is 3.6 × 3.2 mm^2, the micro photo of the chip is reported in Fig. 5. It absorbs 17.6 mA from 3.3 V. The DVCO core uses 9.6 mA, the remaining current is mainly absorbed by the output buffer. The prototype has been designed for oscillating in four different bands. The first band is centered around 900 MHz, the second one around 1.5 GHz, the third one around 1.8 GHz and the last one around 2.4 GHz.

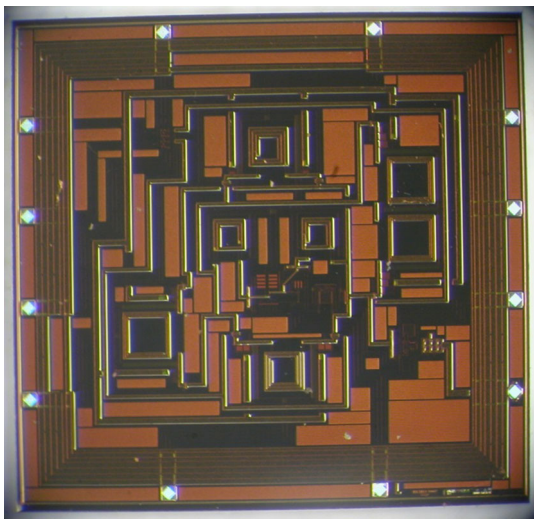

Fig. 5 Micro photo of the DVCO

Inside the DA, the π-cell topology has been used to reduce the number of inductors. To separate the bias network from the signal path, MIM (Metal–Insulator–Metal) capacitances have been used instead of poly–poly capacitances not only for the higher Q factor but primarily for the achievable big reduction of the bottom plate-well/substrate parasitic capacitance. This latter has the same unwanted effect of the parasitic components of the inductors and it can lead to a reduction of the band of synthesis.

The switched-cells structure used to design the SL is the parallel configuration of Fig. 4(a) with four branches each one governing one of the four wanted bands. This implementation uses more area than the cascade topology but it simplifies the matching design and represents a simpler way to test this tuning scheme.

The device has been designed and simulated by using Cadence and the simulated performances in the four bands are summarized in Table 1. Simulated phase noise and harmonics suppression are good and uniform along the tuning ranges. The post-layout simulations provide optimum results in terms of tuning range confirming the theory.

The specs adopted for the design define quite wide subbands and the use of abrupt varactors in each cell of the SL allows to meet the requirements. Actually the process variations could introduce a sensible dc offset which, in turn, would shift the effective tuning characteristic C(V) provided by the abrupt varactors causing a reduction of the synthesized tuning range. To manage this problem, the reported circuit adopts a switched bank of varactors able to better control the effective C(V) provided by each cell even in case of dc offset. An accurate Montecarlo analysis has been performed and finally the DVCO has been fabricated.

Table 1 Simulations results of the multi-band IC DVCO based on the switched cells tuning technique

	Tuning range (MHz)	TR (%)	Output power Min/Max (dBm)	2° Harmonic suppression Min/Max (dBc)	3° Harmonic suppression Min/Max (dBc)	Phase noise @1 MHz offset Best/Worst (dBc/Hz)
Sub-band 1	745–1044	33.4	−8.5/−5.5	27/38	35/52	−123/−107
Sub-band 2	1324–1692	24.4	−7.3/−7.0	34/45	34/45	−116/−104
Sub-band 3	1580–2038	23.3	−8.5/−7.8	25/33	31/44	−118/−103
Sub-band 4	2290–2560	11.1	−10.5/−9.3	27/31	31/33	−110/−104
All Sub-bands	745–2560	84.4	−10.5/−5.5	25/45	31/52	−123/−103

The output synthesized by the prototype has been measured with a spectrum analyzer, Agilent E4407B. The measured tuning ranges are reported in Fig. 6 compared with the simulations in each sub-bands. All the measured sub-bands are smaller than the simulated one and the agreement is not perfect but acceptable.

In Fig. 7 the phase noise at the at the upper band limit of the sub-band 1 is reported. The phase noise measurements in all sub-bands have been estimated by using the following equation:

$$L(fm) = L(fm)_{measured} - 10\,log_{10}(RBW) \quad (15)$$

where *fm* is the frequency offset and RBW is resolution bandwidth used for the measurement.

In Table 2 the measurements are summarized. The harmonic suppression and phase noise have been measured in 15 values of frequency for each sub-band.

The phase noise measurements pointed out a deterioration in correspondence of the upper limit of each sub-band. Probably, this is due to the different effectiveness of the filtering introduced by the SL, as predicted by the theoretical analysis. Indeed this latter is slightly more effective for frequencies of oscillation close to the lower edge of the range of synthesis.

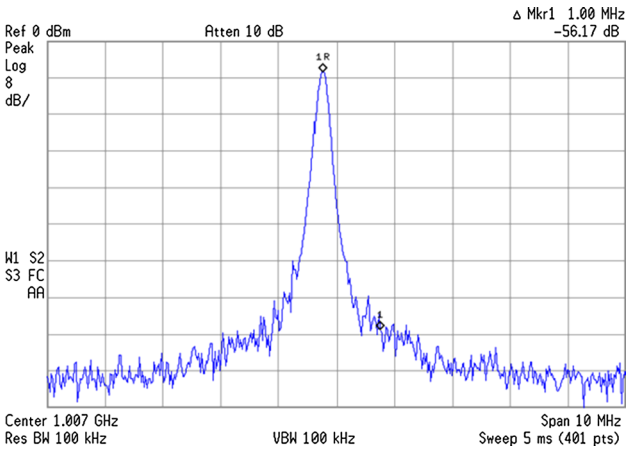

Fig. 7 Phase noise at the upper band limit of the sub band 1

In Table 3 are reported the measurements of similar DVCOs found in literature and operating in forward gain mode.

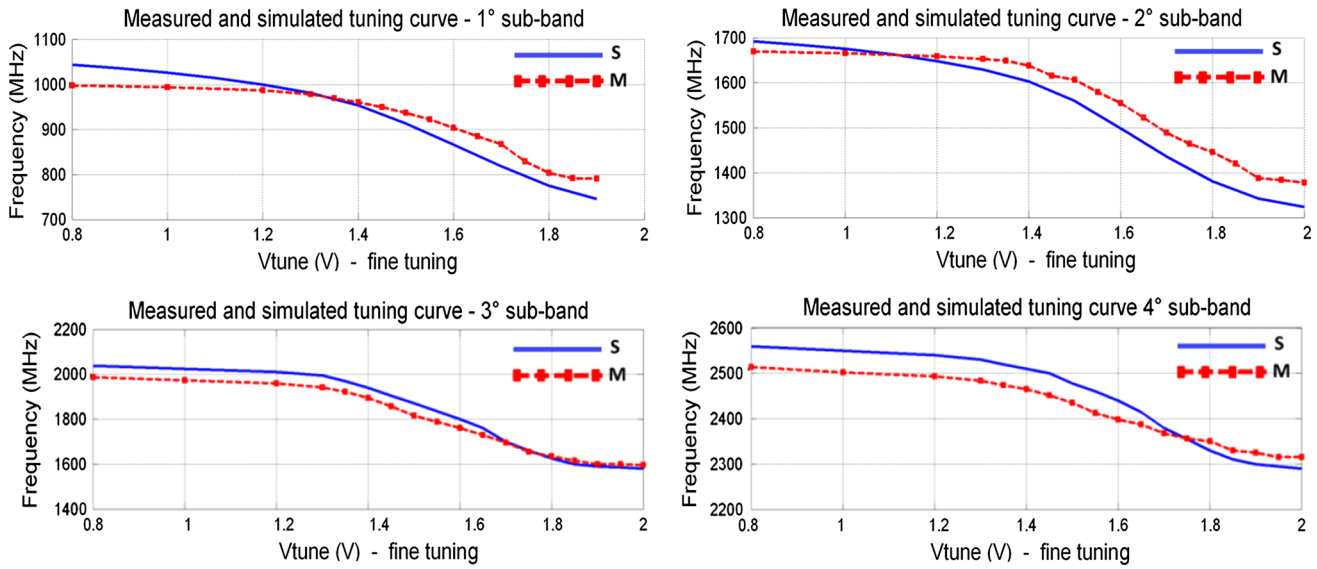

Fig. 6 Comparison between measured and simulated tuning characteristics for the 4 sub-bands

Table 2 Measurement results of the multi-band IC DVCO based on the switched cells tuning technique

	Tuning range (MHz)	TR (%)	Output power Min/Max (dBm)	2° Harmonic suppression Min/Max (dBc)	3° Harmonic suppression Min/Max (dBc)	Phase noise @1 MHz offset Best/Worst (dBc/Hz)
Sub-band 1	791–1010	24.3	−9.2/−4.5	24/36	28/36	−106.18/−96.44
Sub-band 2	1378–1669	19.1	−8.5/−7.3	24/38	28/37	−105.57/−92.09
Sub-band 3	1595–1987	21.9	−9/−8.2	24/32	29/40	−105.99/−93.18
Sub-band 4	2315–2514	8.2	−10.9/−9.7	25/29	28/30	−105.63/−92.57
All sub bands	791–2514	65.9	−10.9/−4.5	24/38	28/40	−106.18/−92.09

Table 3 Measurement results of Distributed VCOs in forward gain mode

References	Tuning range	TR (%)	Phase noise	Power supply	Technology
[13]	9.5–10.4 GHz (CMOS)	9	−103dBc/Hz @600 kHz	35 mW	BiCMOS
	10.6–12 GHz (Bipolar)	12.4	−99dBc/Hz @600 kHz	15 mW	0.35 um
[15]	13.95–14.37 GHz	3	−98dBc/Hz @1 MHz	138.1 mW	SiGe BiCMOS 0.35 um
[16]	10.6–11.7 GHz	9.8	−116dBc/Hz @1 MHz	72 mW	CMOS 65 nm
[17]	12–12.17 GHz	1.4	−115.16dBc/Hz @1 MHz	108mW	CMOS 0.18 um
[18]	4.97–5.46 GHz (injection locked)	9.4	−121dBc/Hz @1 MHz	39.15 mW	PCB
[20]	8.2–9.8 GHz	17.7	−103dBc/Hz @1 MHz	100 mW	SiGe BiCMOS
[This work]	0.79–2.5 GHz	65.9	−106.18 @1 MHz	31.7 mW	BiCMOS 0.35 um

Measurements demonstrated that the proposed technique achieves a wider tuning range compared to previous implementations while providing uniform performances. Moreover, the proposed approach can be easily frequency scaled furnishing a powerful solution even for mm-wave applications.

5 Conclusions

As expected from theory, the experimental results for the proposed DVCO demonstrate good performances in terms of wide tuning range, phase noise, and harmonics suppression.

The key advantages of the proposed structure reside in the availability over a wide bandwidth of a gain-tank and the concurrent possibility to implement the "switched-cells tuning technique". This represents an optimum starting point to design a wideband VCO like those required by modern advanced transceivers.

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