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GUEST EDITORIAL

Special Issue on Advances in sensing and communication circuits (ICECS 2012)

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This special issue includes 15 papers selected from some 250 presented at the 2012 International Conference on Electronics, Circuits and Systems (ICECS 2012) held December 09–12 in Seville, Spain. ICECS 2012 got 380 submissions from 51 different countries; 69.7 % of the papers came from IEEE Region 8, while the rest came from the other IEEE regions. Selection of the papers for this special issue was based on: (1) the feedback of the audience; (2) the feedback of the session chairs; and (3) the scores given by the ICECS TPC members. Selected papers were invited to submit extended versions on early March 2013. All papers were peer reviewed. Papers in the issue have been organized into different section covering topics related to the general theme of sensing and communication circuits and systems. The papers are briefly introduced in the sections below.

1 Sensors and sensory systems

This paper by D. Jiang and A. Demosthenous deals with the merging topic of implantable neuro-prosthetic systems. It provides a review of the development in vestibular prostheses to date, and uses a specific example to demonstrate the problems in designing the implantable circuits for such systems. M. Carminati et al. addresses the topic of molecule detection by using solid-state nano-pores. The final goal is label-free high-throughput DNA sequencing. The paper presents a new two-channel current amplifier tailored for solid-state nanopore devices with integrated tunneling electrodes, analyzes different design trade-offs and show results for a lamda-DNA platform with 20 nm pores. A. Alfaifi et al. presents a $1 \times 1\text{-mm}^2$ dual-axis accelerometer fabricated in a SOI process plus an in-house back-end release step. Experimental results are reported: average cross sensitivity of ~ 0.87 % with ~ 101 'digital counts'/g, that is, 16.83 fF/g in both axes, X and Y. A remarkable feature of this device is that rotational motion and Z accelerations have no impact on the X and Y readings. This is due to the particular geometry of the device. The paper by M.A. Paun et al. evaluates the temperature effects on the current-related sensitivity of Hall-Effect sensors. An analysis of the carrier concentration temperature dependence is carried out and experimental results are presented for the sensitivity and input resistance temperature dependence. The section is closed by the paper from A. Salazar et al. It presents simulation results obtained along different design stages of a biosensing platform based on Surface Plasmon Resonance (SPR) and incorporating a CMOS imager. Specifically, a numerical analysis to determine the optimal plasmon resonance conditions is reported. A numerical analysis to select the best CMOS photodiode is also described. Finally, the architecture of the corresponding CMOS imager is proposed. As a whole, this work gathers valuable information required for the successful implementation of a SPR-biosensing platform incorporating a CMOS Active Column Sensor.

2 CMOS image and radiation sensors

The first paper in this section, by L. Mereni et al. is devoted to circuits for passive radiometry Specifically, the paper

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address a study on the feasibility of W-band passive radiometers in nanoscale CMOS technology for imaging applications. The study takes into account some of the most relevant aspects regarding the system-on-a-chip implementation, from system to circuit and technology limitations, with emphasis on the impact of the non-idealities of the detector on the overall system performances. S.J. Carey et al. report a vision chip based on a 20×64 mixed-signal processing array. This array features elementary cells containing a photodetector, an ALU and digital and analog memory. One of the main advantages of this circuitry when arranged as a processing lattice is that the array can be configured for asynchronous propagation, enabling ultra-high-speed operations like flood filling. Applications working at 30,000 frames per second are presented. The paper by S. Vargas-Sierra et al. reports an algorithm for acquisition of high dynamic range images. This algorithm applies the same tone mapping curve to all pixels, adapting itself dynamically to the contents of the scene. Experimental results based on a smart QCIF CMOS imager are provided. These results demonstrate the suitability of the proposed technique to compress HDR images while keeping details and contrast information for subsequent post-processing.

3 Communication circuits and systems

This section starts with the paper by M.P. Kennedy et al. that propose two variants of LC CMOS injection-locked frequency dividers that can operate equally well in both divide-by-2 and divide-by-3 modes. The circuits presented in this work are implemented with only one integrated inductor and designed in a 65 nm CMOS technology to operate within the multi-GHz frequency range. F.A. Bakar et al. present the design, implementation and experimental characterization of the analog part of an integrated receiver intended for Synthetic Aperture Radar applications. The receiver—which includes a three-parallel-signal channel RF front-end, a reconfigurable analog baseband chain with 50/160 selectable bandwidth, and a 8-bit ADC—has been fabricated in a 130 nm CMOS technology with 1.2-V supply voltage, featuring a reconfigurable nominal gain of 40/37 dB and a noise figure of 11/13.5 dB for L-band and C-band, respectively. The maximum power consumption is 650/800 mW with a 50/160 MHz baseband filter, respectively. In the last paper of this section, S.M. Safavi and M. Shabany introduces a novel multiple antenna, high-resolution eigenvalue-based spectrum sensing algorithm based on the FFT of the received signal. A real-time, low-area, and low-power VLSI architecture is developed for the proposed algorithm, which is implemented in a 180 nm CMOS technology. This design constitutes the first eigenvalue-based detection architecture proposed to date, capable of detecting weak signals at -10 dB, occupying a total area of 3.4 mm^2, and dissipating 78 mW for a 32-subchannel 40 MHz sensing bandwidth.

4 Design of analog front-end circuits

The first paper of this section, by T. Watanabe and T. Terasawa, reports an all-digital 6- to 16-bit adaptive time A/D converter applied to high-resolution low-power sensor/RF interfaces. Minimum/maximum detectable sensitivity of 0.7 μVrms/100 mVrms is experimentally achieved in a 0.18 μm CMOS process. The ultimate objective of the proposed approach is making sensor/RF ADCs more compact and scalable while easing their design and test thanks to the all-digital nature of the circuitry. B. Sedighi et al. addresses the problem of optimizing area occupation and power consumption of SAR ADCs under noise performance constraints. The paper shows that parasitic capacitances and ON-resistances of the switches play an important role in the noise performance and analyse different hybrid resistive-capacitive DACs seeking for improvements in energy efficiency. T. Rabuske et al. present two improved comparator-based binary-search ADC architectures for UWB receivers. The first ADC topology uses 2N-1 comparators arranged in N stages, and the second one uses only N threshold-reconfigurable comparators arranged one per stage. These two circuits are designed in a 90 nm CMOS technology to operate at 1.5 GS/s, achieving a resolution of 4-bit and 5-bit, respectively, for a 1-V input signal range, with a single 1-V supply voltage. The last, but not the least, paper in the issue, by A. Buonomo and A. Lo Schiavo addresses the topic of analog modelling for equation-based design. Specifically, the paper derives closed-form expressions to predict nonlinear distortion in analog integrated circuits with application to GmC filters and nested Miller compensated opamps.

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