Continuous-time delta-sigma modulator using vector filter in feedback path to reduce effect of clock jitter and excess loop delay

Yuki Kimura · Akira Yasuda · Michitaka Yoshino

Abstract In this paper, we propose a novel delta-sigma modulator (DSM) that reduces the effects of clock jitter and excess loop delay by using a vector filter in the feedback path. The vector filter divides the input signal into a high-frequency part and a low-frequency part. The low-pass signal is placed in the path to the first-stage digital-to-analog converter for reducing the effects of the clock jitter, and the high-pass signal is placed in the feedback path to the last integrator in order to compensate for the excess loop delay. The DSM using the vector filter in the feedback path (DSM-VF) is verified using MATLAB/Simulink. Further, a clock jitter (0.1 %) in DSM-VF leads to an improvement in the signal-to-noise-ratio (SNR) to 22.5 dB as compared to the SNR of a conventional CTDSM. Moreover, the SNR deterioration caused by the excess loop delay is improved.

Keywords Analog-to-digital converter (ADC) · Continuous-time delta-sigma modulator (CTDSM) · Vector filter · Clock jitter · Excess loop delay

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1 Introduction

In the recent years, the use of complementary metal-oxide semiconductor (CMOS) miniaturization technology has led to improvements in the digital circuit used in electrical equipment. These improvements have led to a considerable increase in the demand for high-speed, high-precision analog-to-digital converters (ADCs) in order to leverage the advanced digital circuit technology. Delta-sigma modulators (DSMs) are widely used as high-precision, low-speed ADCs [1–3]. Recently, continuous-time delta-sigma modulators (CTDSMs) have been utilized for high speed applications because their high-speed operation is easier than that of a discrete-time implementation such as a switched capacitor circuit. The demand for element circuits used for constructing CTDSMs is lower than that for discrete-time delta-sigma modulators (DTDSMs). However, there is drawback related to the use of CTDSMs: the signal-to-noise-ratio (SNR) of CTDSMs deteriorates because of the clock jitter and the excess loop delay. In this paper, a novel DSM with a vector filter simultaneously realizing a low-pass and high-pass filter in the feedback path (DSM-VF) is proposed in order to improve the effects of the clock jitter and the excess loop delay.

The paper is organized as follows: Sect. 2 explains a disadvantage of CTDSM. Section 3 discusses the proposed method. In Sect. 4, a design method of the proposed system is explained, and Sect. 5 presents the simulation result of the proposed system. Section 6 shows a circuit design plan. Furthermore, the effect of the current mismatch caused by the variation of the transistor performance is explained. The latter half of the section verifies the influence of variations and mismatches of multi-bit DAC followed by the conclusion in Sect. 7.

2 Problems of CTDSM

2.1 Clock jitter

Clock jitter refers to the timing variations of a set of signal edges from their ideal values. The clock jitter deteriorates the performance of digital-to-analog converters (DACs). The degradation for the CTDSM is considerably larger than that for the DTDSM. This is because a current-steering DAC and a switched-capacitor DAC are usually used for CTDSM and DTDSM, respectively. The output current of the DACs is shown in Fig. 1. The influence of the clock jitter on the DAC of the CTDSM is considerably larger than that in the case of DTDSM since the output current of the DAC of the CTDSM is constant at the clock edge.

From a different point of view, the clock jitter phase modulates the output of the DAC signal. Therefore, the random clock jitter down-converts the quantization noise shaped at a relatively high frequency by the DSM to the signal band. As a result, the noise floor in the signal band increases.

2.2 Excess loop delay

Excess loop delay is a delay that occurs in a comparator, a flip–flop circuit, and the DAC. The main causes of the excess loop delay are time-constant and the slew rate limit of the circuits.

When CTDSM is designed, the loop is designed considering the expected delay time. However, if the excess loop delay increases to a value more than the estimated value after fabrication, the DSM becomes unstable.

3 Proposed methods

3.1 Vector filter

The vector filter simultaneously realizes a low-pass and a high-pass filter. One clock delay exists between the inputs
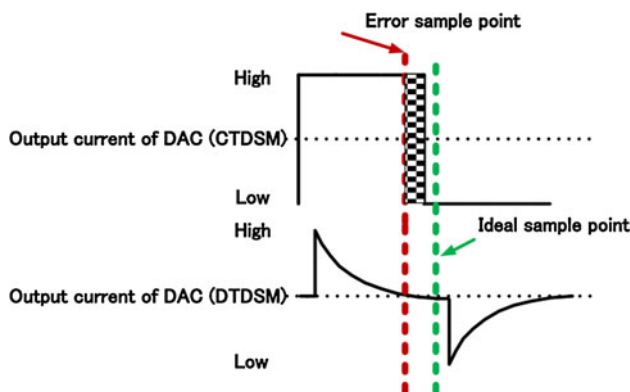

Fig. 1 Output current of DAC (CTDSM and DTDSM)

of the vector filter, as shown in Fig. 2. Output Y_L and Y_L are as follows:

$$
\begin{aligned}
\begin{pmatrix} Y_L \\ Y_H \end{pmatrix} &= \begin{pmatrix} 0.5 \\ 0.5 \end{pmatrix} \begin{pmatrix} 1 & 1 \\ -1 & 1 \end{pmatrix} \cdot \begin{pmatrix} X \\ z^{-1} \cdot X \end{pmatrix} \\
&= \begin{pmatrix} 0.5X \\ -0.5X \end{pmatrix} \cdot \begin{pmatrix} 1 + z^{-1} \\ 1 - z^{-1} \end{pmatrix}
\end{aligned} \tag{1}
$$

$$
\begin{pmatrix} Y_L \\ Y_H \end{pmatrix} = \begin{pmatrix} 0.5X \\ -0.5X \end{pmatrix} \cdot \begin{pmatrix} 1 + z^{-1} \\ 1 - z^{-1} \end{pmatrix}
$$

Paths of Y_L and Y_H have the low-pass and high-pass characteristics, respectively. The vector filter is conventionally used for a time-interleaved delta-sigma modulator (TIDSM) [4]. In this study, a vector filter is used for realizing the characteristics of a low-pass and high-pass filter in a feedback path simultaneously. The system of the conventional second-order CTDSM is shown in Fig. 3. The DSM using the vector filter in the feedback path is shown in Fig. 4.

The proposed method can improve the noise performance deteriorated by a clock jitter and a stability degraded by an excess loop delay. Furthermore, it is possible to keep the bit-length of an internal ADC single-bit. Using a multi-bit internal ADC is well known as the conventional method to reduce the influence of jitter. However, the multi-bit ADC increases the number of comparators, and the hardware is large. Additionally, using the multi-bit ADC, the delay time of the entire ADC sometimes increases. In recent years, the low power-supply voltage is demanded by advanced CMOS technology. The low-bit internal ADC makes the circuit realization easy. Therefore, we choose the proposed method using the vector filter in this paper.

3.2 Low-pass signal to reduce clock-jitter effect

The influence of the clock jitter of DAC1 is the largest in Fig. 3. Because, the noise to be added to the feedback signal of the first integrator caused by clock jitter appears at the output of ADC. The influence of clock jitter is reduced by the low-pass filter realized by a vector filter in the DAC1 path. The output signal of this low-pass filter is added to the first integrator. The low-pass filter has a notch at the Nyquist frequency, since the quantization noise is large at this frequency (Fig. 5).The low-pass filter by the
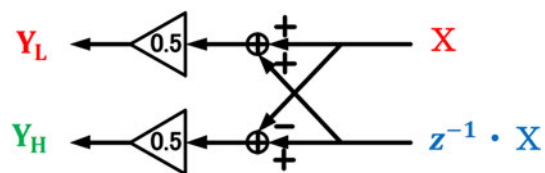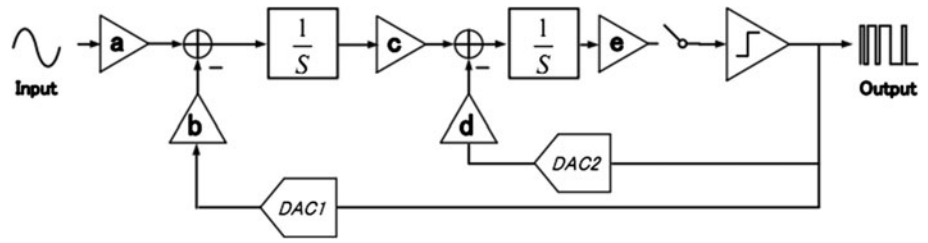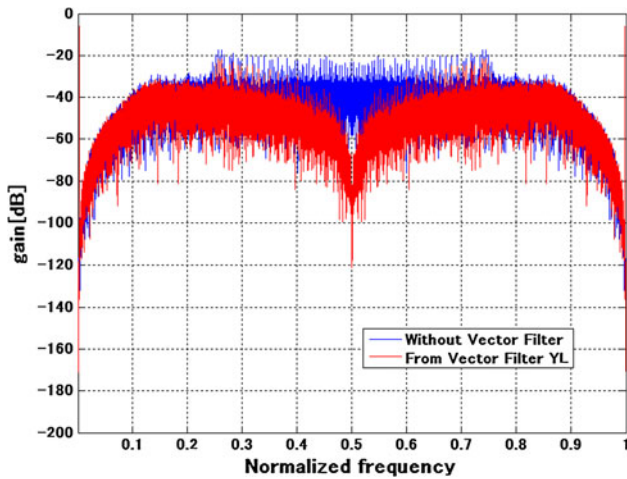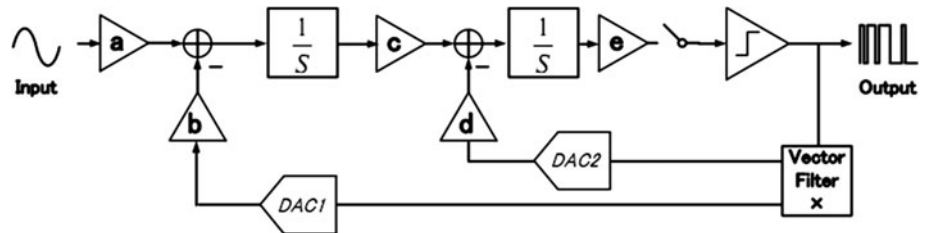

Fig. 2 Vector filter

Fig. 3 Conventional second-order CTDSM

Fig. 4 DSM using vector filter in feedback path

Fig. 5 Output spectrum of feedback path with low-pass filter using vector filter

vector filter reduces the quantization noise at the high frequency. This reduces the SNR deterioration by clock jitter [5]. Because, the quantization noise to be down-converted to the signal band from the high frequency by clock jitter is reduced (Fig. 6). Furthermore, removing the high frequency quantization noise, the amplitude change between one clock periods becomes small, which reduces the influence of the jitter (Fig. 7).

3.3 High-pass signal versus excess loop delay

Figure 4 shows that the vector filter adds a high-pass signal in the feedback path to the last integrator. The high-pass signal realizes phase compensation in the feedback path. The local feedback path can reduce the phase lag at a high frequency.

If a low-pass filter is used in feedback path for reducing effect of clock jitter without the high-pass signal, the influence of excess loop delay is larger than conventional

CTDSM. However, the high-pass signal can improve the influence of excess loop delay.

4 Design of proposed CTDSM

4.1 Design using discrete-time model

The design using a discrete-time model (DT model) is used because there is a significant amount of information available on the discrete-time DSM.

The DT model of the proposed system is shown in Fig. 8. This system has coefficients "c" and "d" for comparison with the conventional system shown in Fig. 3 in order to locate the poles at the origin.

The transfer function of the DT model is expressed as follows:

$$Y = z^{-1}X + z^{-2}(1 - z^{-1})^2 Q. \tag{2}$$

where Y is the output of the modulator, X is the input of the modulator, and Q is the quantization noise.

The DT model of the proposed system is simulated. The simulation result is shown in Table 1 and Fig. 10. The second-order noise-shaping-characteristic is clearly observed in Fig. 10.

4.2 Conversion from DT model to CT model

Bilinear transform is a method used for converting the DT model into the CT model. The CT model is converted from the DT model shown in Fig. 8 by using a bilinear transform. The CT model equivalently converted by the bilinear transform is shown in Fig. 9. The simulation result of the DSM-VF (CT model) is shown in Fig. 10 and Table 2. Table 2 and Fig. 10 reveal that the DT model and the CT model exhibit equivalent noise shaping and SNR characteristics.

Fig. 6 Comparison of jitter influence for quantization noise between system with/without vector filter. (Fs is sampling frequency)
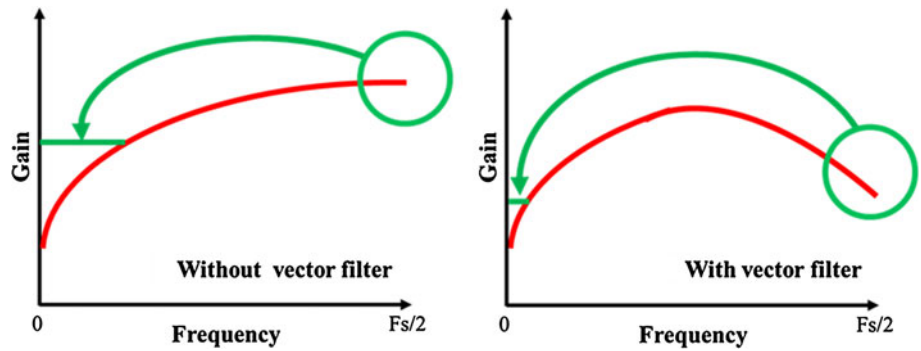
4.3 Confirmation of low-pass and high-pass characteristics

The output spectrum of the vector filter toward DAC1 and DAC5 is shown in Fig. 11. Figure 11 shows that the low-pass signal has a notch at the Nyquist frequency.

Next, the output spectrum of the vector filter toward DAC2 is shown in Fig. 12. The third-order noise shaping is observed because the output of DSM-VF (CT model) with second-order noise-shaping characteristics is the input of the vector filter and the vector filter has a first-order high-pass characteristics.

Figures 11 and 12 can confirm that the vector filter exhibits low-pass and high-pass characteristics on the feedback path.
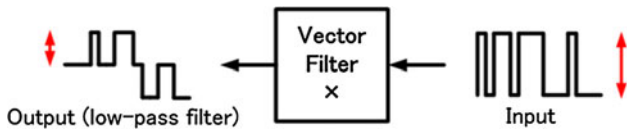
Fig. 7 The output amplitude change of low-pass filter by vector filter

## 5 Simulation result of DSM-VF with clock jitter and excess loop delay

5.1 The explanation of jitter model

The jitter model used in MATLAB/Simulink is shown in Fig. 13. The clock with jitter is generated by the clock-generator, white-noise generator and variable time delay block. The clock-generator generates the ideal clock. (Ts is the ideal sampling period). The white-noise generator
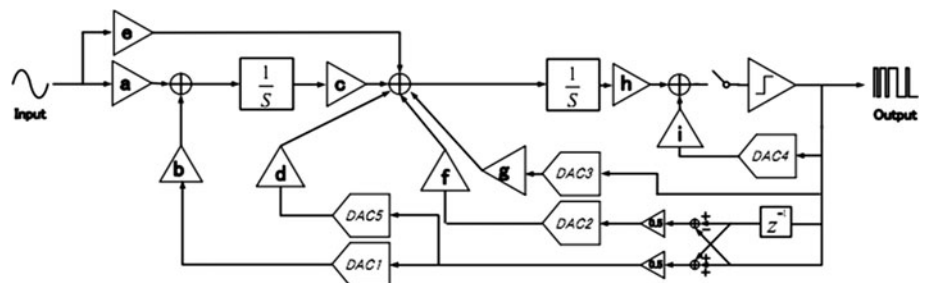
Table 1 Simulation result of DT model

Parameters	Measurement results (DT model)
Input level	−6 (dBFs)
Sampling frequency (normalized)	1 (Hz)
Oversampling ratio	128
Plot	2^{15}
Signal-to-noise ratio	85.2 (dB)
Effective number of bits	13.9 (bit)

Fig. 8 Discrete-time model of DSM-VF
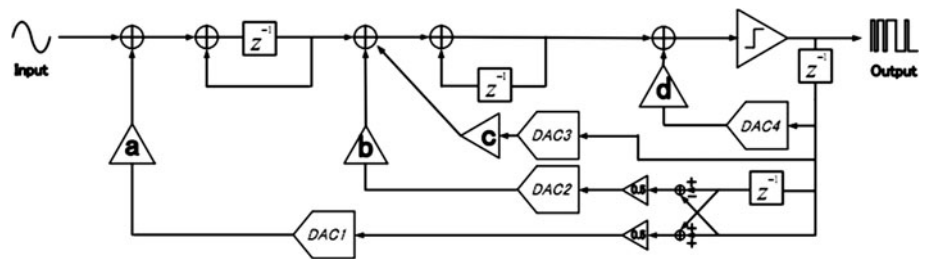
Fig. 9 Continuous-time model of DSM-VF

generates a bandlimited whitenoise (Fig. 14). The bandlimited whitenoise outputs normally distributed random numbers where average and variance are zero and one, respectively. The strength of jitter is determined by the amplitude of bandlimited whitenoise. In this paper, the strength is set to 0.1 % of the clock period. The variable time delay adds the delay time to the ideal clock from $T_s - \Delta T_j$ to $T_s + \Delta T_j$ according to In2. ΔT_j is the delay
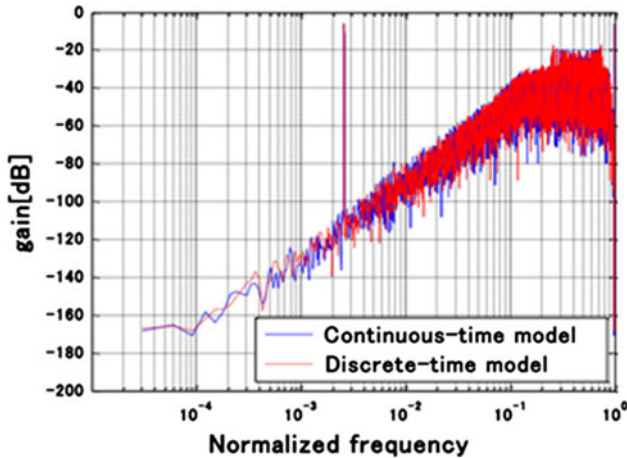

Fig. 10 Output spectrum of DT model and CT model

Table 2 Simulation result of CT model

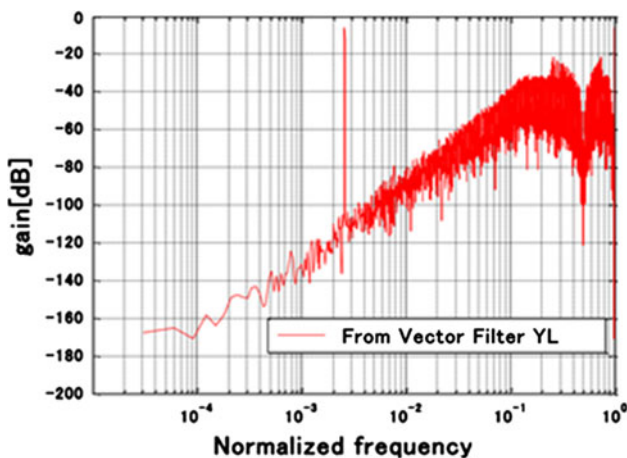| Parameters	Measurement results (CT model)
Input level	−6 (dBFS)
Sampling frequency (normalized)	1 (Hz)
Oversampling ratio	128
Plot	2^{15}
Signal-to-noise ratio	84.8 (dB)
Effective number of bits	13.8 (bit)

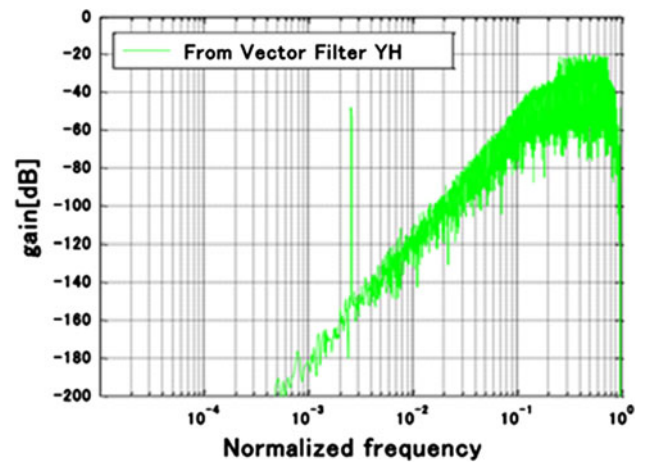Fig. 11 Frequency spectrum of path toward DAC1 and DAC5 shown in Fig. 9

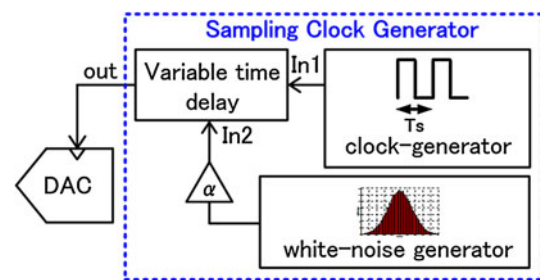Fig. 12 Frequency spectrum of path toward DAC2 shown in Fig. 9
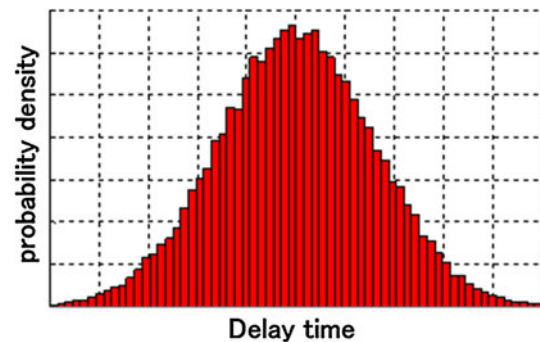

Fig. 13 Clock jitter model

Fig. 14 Generated delay time by white-noise generator

Table 3 Simulation results of conventional and DSM-VF

Parameters	Conventional	DSM-VF (CT model)
Clock jitter	0.1 (%)	0.1 (%)
Input level	−6 (dBFS)	−6 (dBFS)
Sampling frequency (normalized)	1 (Hz)	1 (Hz)
Oversampling ratio	128	128
Plot	2^{15}	2^{15}
Signal-to-noise ratio	61.7 (dB)	84.2 (dB)
Effective number of bits	10.0 (bit)	13.7 (bit)

time for jitter. When the influence of clock jitter is verified, the clock jitter model is used at DAC1, 2 in Fig. 3 and DAC1, 2, 3, 4, 5 in Fig. 9.
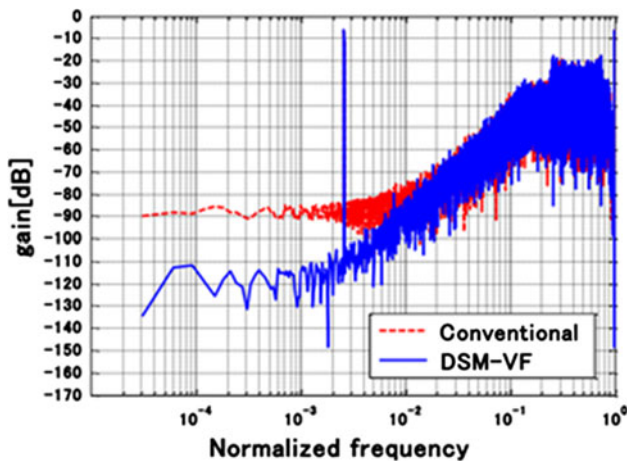

Fig. 15 Comparison of clock jitter (0.1 %) effect between conventional and DSM-VF
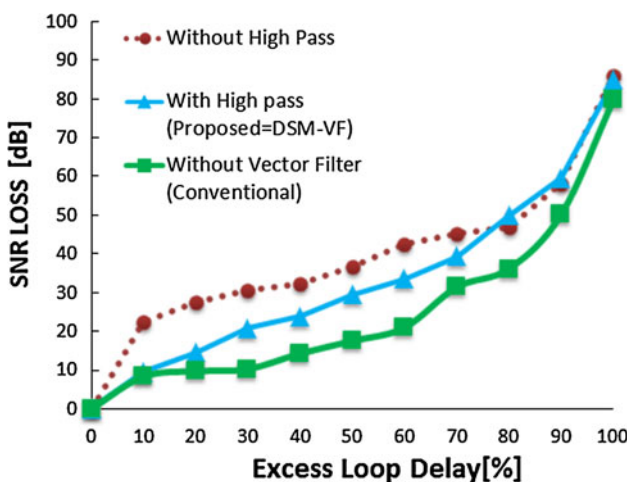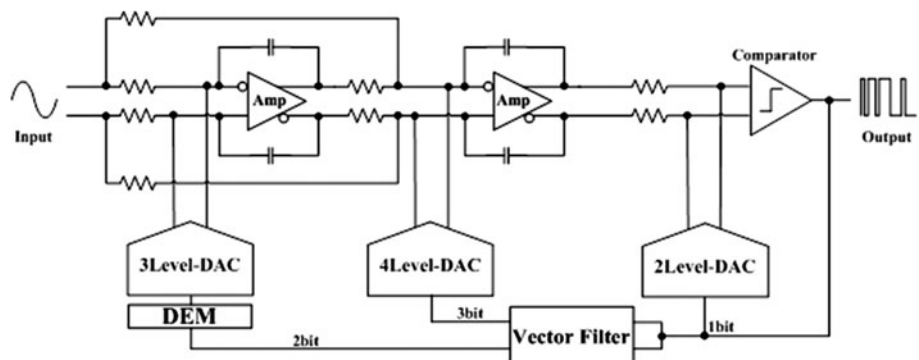

Fig. 16 Comparison of excess-loop-delay effect system without high-pass filter, DSM-VF and conventional

5.2 Comparison of clock jitter effect

The clock jitter is applied to the conventional CTDSM shown in Fig. 3 and the DSM-VF (CT model) shown in Fig. 9. The simulation results and the output spectrums are shown in Table 3 and Fig. 15, respectively. The clock jitter is a 0.1 % random jitter.

Table 3 and Fig. 15 show that SNR is improved by 22.5 dB

5.3 Comparison of excess loop delay

The proposed system is compared with a system that does not use a high-pass filter. All the poles of both the systems are located at the origin. Therefore, the systems have the same stability. The SNR deterioration due to the excess loop delay in systems with/without a high-pass filter is shown in Fig. 16.

The horizontal axis is the ratio of the excess loop delay in Fig. 16. When the excess loop delay is 0 % of the sampling period, the SNR values for both the systems are almost the same. If the excess loop delay is <70 % of the sampling period, the SNR deterioration of the DSM-VF with a high-pass filter is approximately 10 dB less than that for the system without a high-pass filter. When the low-pass filter is used in feedback path to reduce the effect of the clock jitter, there is the problem that the influence of excess loop delay is larger than conventional CTDSM. However, the high-pass filter can improve the influence of excess loop delay to conventional CTDSM.

6 Design plan and the effect of variations and mismatches

### 6.1 Design plan (circuit domain)

The vector filter is realized by digital circuits. The bit length of the vector filter becomes several-bit by using the adder and subtractor. The number of elements constructing

Fig. 17 Design plan (circuit domain)

Table 4 The influences of the absolute gain variation

3 Level-DAC mismatch (%)	4 Level-DAC mismatch (%)	2 Level-DAC mismatch (%)	SNR (dB)
0	0	0	84.8
10	0	0	84.5
−10	0	0	86.7
0	10	0	84.8
0	−10	0	85.4
0	0	10	85.4
0	0	−10	85.9
10	10	10	85.3
−10	−10	−10	86.1
10	−10	−10	83.6
−10	10	−10	85.6
−10	−10	10	86.5
10	10	−10	84.6
−10	10	10	86.6
10	−10	10	85.1

Table 5 The influences of the relative current mismatches

3 Level-DAC mismatch (%)	4 Level-DAC mismatch (%)	2 Level-DAC mismatch (%)	SNR (dB)
0	0	0	84.8
±1	0	0	60.1
0	±1	0	83.4
0	0	±1	86.0
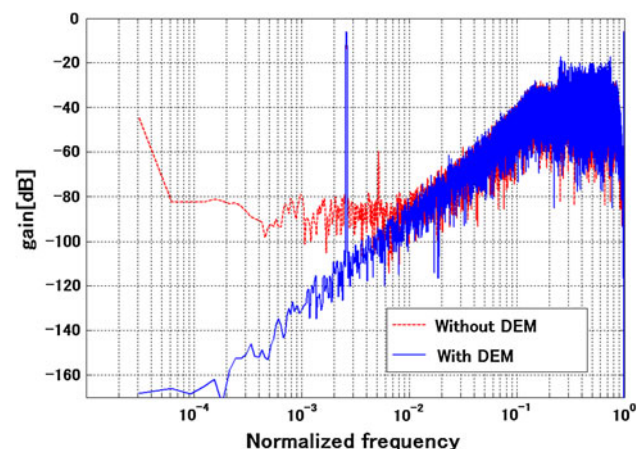
Fig. 18 Comparison of relative variability of ±1 % effect between system without DEM and with DEM

the DAC is increased by the bit length of the vector filter. The mismatch among the elements implementing current source causes nonlinear effects. The dynamic element matching (DEM) circuit is placed in the path to the

Table 6 Simulation results of proposed ADC without DEM and with DEM

Parameters	Without DEM	With DEM
Relative current mismatches	±1 (%)	±1 (%)
Input level	−6 (dBFs)	−6 (dBFs)
Sampling frequency (normalized)	1 (Hz)	1 (Hz)
Oversampling ratio	128	128
Plot	2^{15}	2^{15}
Signal-to-noise ratio	60.1 (dB)	84.8 (dB)
Effective number of bits	9.7 (bit)	13.8 (bit)

first-stage DAC to reduce the nonlinearity effect of the mismatch. The final circuit design plan is shown in Fig. 17.

6.2 The effect of absolute gain variations and relative current mismatches of DAC

The DAC to the same terminal can be realized by the single DAC (Figs. 9 and 17). The bit length of this DAC is increased. The DAC is realized by a current-steering DAC. However, the absolute value of the current is varied by the variation of threshold voltage and mobility. Therefore, the absolute gain variation of the current-steering DAC is about 10 %. Furthermore, there is the relative current mismatch 1 % among current cells of the DAC. The influence of the variations and mismatches is verified by simulation using MATLAB/Simulink. The DACs concerning about current variation are three-level DAC, four-level DAC and two-level DAC in Fig. 17. The influences of the absolute gain variation of three-level DAC, four-level DAC and two-Level DAC are shown in Table 4. The influences of the relative current mismatches of three-level DAC, four-level DAC and two-level DAC are shown in Table 5. Table 4 shows that the influence of absolute gain variations is small. The relative current mismatches of three-level DAC deteriorate the SNR (Table 5). However, the DEM can improve the influence of the relative current mismatches (Fig. 18 and Table 6).

7 Conclusion

We propose a novel CTDSM using a vector filter that simultaneously realizes low-pass and high-pass characteristics in the feedback path and confirm that the DSM-VF reduces the SNR deterioration caused by the clock jitter and the excess loop delay. The influence of the absolute gain variation and the relative current mismatches of the DAC are simulated by MATLAB/Simulink. The robustness of the proposed system for those variations and mismatches is verified by the simulation. The proposed CTDSM can

achieve a high-precision, high-speed operation. It is assumed that this research will expand application possibility of CTDSM.

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