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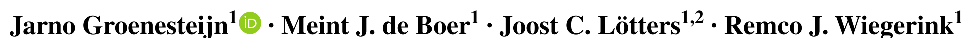
RESEARCH PAPER

A versatile technology platform for microfluidic handling systems, part II: channel design and technology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Abstract Microfluidic devices often require channels of a specific size and shape. These devices are then made in a fabrication process that is often specialized to produce only those (and very similar) channels. As a result, devices requiring channels of different size and shape cannot easily be integrated on the same chip. This paper presents a method to fabricate microfluidic channels in a wide range of shape and size on the same chip by using a slit pattern through which the channels are etched. The fabrication process to fabricate these channels is discussed in detail, and an empirical model is presented to find the optimal slit pattern for a required size and shape. This part of the paper focusses on the channel design and fabrication. Details on the whole fabrication process and optional functionalization of the channels are presented in part I of this paper.

Keywords Microfluidic · Microfluidic handling system · Fabrication · Microchannel · Modelling

1 Introduction

In Groenesteijn et al. (2017), a platform is proposed to make integrated microfluidic handling systems. Channels with a hydraulic diameter from less than 10 µm to well over 100 µm can be made within the same device while the shape of the cross-sectional area can be tuned to the specific application, both without limiting the options for other integrated devices. The channels can be freely suspended, and top-side, bottom-side and in-plane fluidic interfacing is possible. Transducer structures can be integrated in close proximity to the fluid using suitable materials. In these microfluidic handling systems, many different microfluidic devices can be integrated on the same chip. As a result, these devices are connected with very small internal volumes which allows for fast response times and handling of small sample sizes. Several options are proposed to add functionality to the devices. Some examples of these are: metalization, release of the channels from the bulk or a buried oxide layer to mechanically or electrically isolate parts of the chip or provide buried fluidic channels.

In this paper, we discuss several channel etching methods and look at their applicability in the platform. The full fabrication process is discussed in Groenesteijn et al. (2017). The channels are etched isotropically through etch slits in a silicon-rich silicon nitride layer on top of the wafer. As a result, the size and shape of the channels can be tuned to meet the demands of any application. Here, we propose a method, based on an empirical etch model, to design the slit pattern that will result in the desired channel shape.

In Sect. 4, the channel design of an integrated microfluidic handling system with multiple fluidic sensors is discussed.

2 Fabrication outline

The fabrication of the devices can be roughly divided into three main steps: fabrication of the microchannels, fabrication of the functional structures and fabrication of the fluidic access to the channels. In this section, an outline of the fabrication process is given where channels are etched at

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the top of the wafer, connected to backside fluidic access holes. The fabrication process and possible functionalization steps are discussed in detail in Groenesteijn et al. (2017).

The two columns in Fig. 1 depict a cross section:

1. The left column shows a cross section along the length of a channel that is connected to a backside fluidic access hole at the left side.
2. The right column shows a cross section perpendicular to two channels with different slit patterns.

The process starts with depositing a 500-nm-thick layer of silicon-rich silicon nitride (SiRN) using low-pressure chemical vapour deposition (LPCVD). A 50-nm-thick layer of chromium is sputtered at the front side of the wafer. The etch-slit pattern, which determines the size and shape of the channels, is transferred using photolithography and etched in the SiRN using a directional plasma etch. Using a semi-isotropic SF_6 plasma etch, the silicon is etched through the etch slits (Fig. 1a). The process parameters used for both these etch steps are given in Table 4. The resist and chromium are removed, and a 1 µm thick layer of silicon dioxide (SiO_2) is depositing using LPCVD of tetraethyl orthosilicate (TEOS, $Si(OC_2H_5)_4$, Fig. 1b). This layer is to prevent etching the channels during the etch of the backside fluidic access holes when the holes reach the channels.

The backside access holes are patterned using photolithography and transferred to the SiO_2 and SiRN layers using a directional plasma etch (Fig. 1c). They are then etched through the silicon wafer using deep reactive-ion etching (DRIE). The SiO_2 layer in the channels is used as an etch stop as shown in Fig. 1d. The SiO_2 is removed using a hydrofluoric acid (HF) etch, and a layer of SiRN is deposited using LPCVD to close the etch slits and form the channel wall (Fig. 1e).

Figure 2 shows an SEM image of a channel structure using a varying slit pattern. The image shows an outer cavity, surrounding an inner cavity. Part of the SiRN membrane with the slits is gone due to the breaking of the wafer. The part that remains shows a dense slit pattern at the inside of the outer cavity, resulting in a deep etch. The sparse slit pattern at the outside results in a shallow etch. A small channel with a slit pattern of two parallel rows of rectangular slits leads out of the cavity at the top.

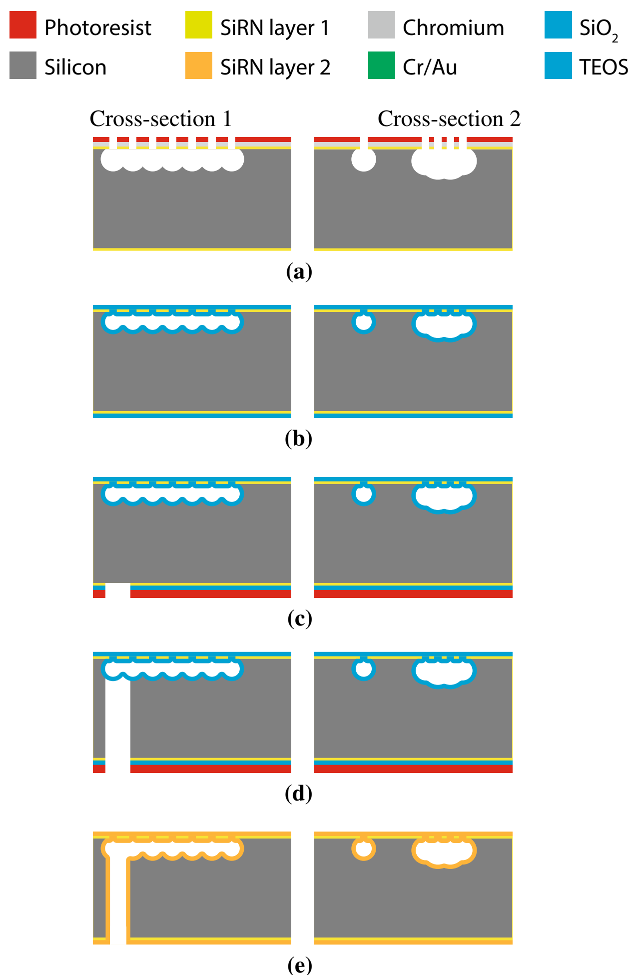

Fig. 1 Fabrication steps to fabricate integrated microfluidic handling systems. The figures are not to scale. **a** Etching of the channels through the etch slits. **b** Deposition of a thick layer of SiO_2 using LPCVD of TEOS. **c** Patterning of the photoresist, SiO_2 and SiRN layers. **d** Etching of the backside access holes through the wafer. **e** Deposition of SiRN to form the channel wall

3 Microchannel technology

Every microfluidic system requires fluid paths, or channels, to achieve the desired functionality and to connect the devices to each other. This means that the ability to easily design their size, shape and layout has a large influence on

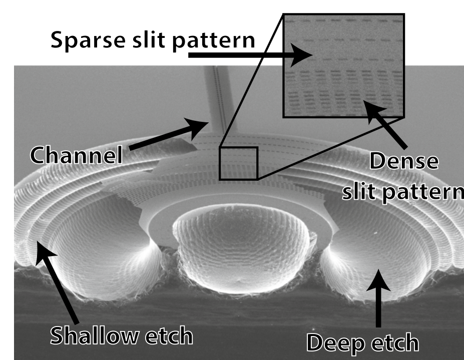

Fig. 2 SEM image showing the effect of the slit pattern density on etch depth in a single etching step

how well they can work for certain applications. The material used to make the channels should be robust enough to prevent leaks or corrosion.

The fabrication of the channels used in Groenesteijn et al. (2017) is presented in detail in this section and can be divided into three parts. First a slit pattern is made to define the layout of the channels. By locally changing the pattern, the cross-sectional size and shape of the channel can be modified to fit a specific purpose. The channels are then etched through the etch slits using a semi-isotropic etch method. Finally, a silicon-rich silicon nitride (Si_xN_y, SiRN) layer is deposited to close the etch slits and to form the channel wall. These steps are shown in Fig. 1.

3.1 Etch-slit pattern

The channels are etched through a slit pattern in a low-stress SiRN layer on top of the silicon wafer. By using slits, the wafer-scale loading during etching is kept low. Even though this reduces the etch rate of the channels, it increases the uniformity of the microchannels over the wafer and defines the etch rate (Tjerkstra 1999). The size of the slits depends on several factors. The slits cannot be made too small to avoid microloading effects (Gottscho Richard et al. 1992). During the processing, we used optical contact lithography to pattern the slits, which also limits the minimum size of the slits. At small sizes, tolerances on the masks and the photolithography, each in the order of ±0.1 µm, will cause relatively large variations in slit size and slit shape, resulting in a variable etch rate through each slit. When a more accurate lithography method is used, the size of the slit can be further reduced as demonstrated by Larsen (2016).

On the other hand, the maximum size of the slits is limited by the SiRN layer which is deposited to form the channel wall and close the slits again. This means that the thickness of the layer is at least half the size of the smallest dimension of the slits. The maximum size of the slits is determined by the maximum desirable thickness of the SiRN layer. Here it should be kept in mind that certain steps in the process might enlarge the slits. For instance, the 50% HF etching step to remove the buried oxide layer when a SOI wafer is used will also etch SiRN at about $4\,\mathrm{nm\,min^{-1}}$. At the top of the channel, the total thickness of the SiRN stack will consist of the initial thin layer and twice the thickness of the layer used to close the slits. When this layer becomes thicker than a few micrometre, the intrinsic stress will cause cracks.

A semi-isotropic etching process is used to etch the channels through the slits; this means that the channels will consist of many connected spheres. Where the spheres connect, the diameter will be less than at the widest part of the spheres, creating scallops. The length of the slits in the direction of the channel and the spacing between two consecutive slits determine the pitch and size of these scallops. In most cases, the scallops should be as small as possible. The size of the scallops is proportional to the spacing between slits, and the spacing determines the minimum size of the etched holes before they form a channel. The pitch of the scallops is proportional to the length of the slits and the spacing. However, very small spacing in relation to the length of the slits will reduce the mechanical strength of the SiRN membrane during etching.Since the size and shape of the slits have such a large influence, it is important to carefully control how they are made. The slits are formed in one of the first steps in the process, as shown in Fig. 1a. This is done by a photoresist layer and a chromium hard mask. Figure 3 shows the influence of the chromium hard mask during several steps in the process. After processing, a horizontal, rectangular cavity is made using focussed ion beam etching to obtain a cross section of the slits. Figure 3a shows a 1.7-µm-thick layer of Olin 907-17 resist after it has been patterned with a 1.2-µm-wide slit. Due to a small taper in the photoresist, the width of the slit at the bottom of the photoresist is about 1.14 µm. The chromium has no influence on this step. Figure 3b shows the results after the SiRN has been etched. In the case shown with chromium, the SiRN has not been fully etched through. The photoresist has approximately the same taper as before the etch and some chromium has re-deposited onto the side walls. The width of the slit at the top of the SiRN is 1.24 µm, due to a small taper in the SiRN, the width is slightly smaller at the bottom of the SiRN: 0.96 µm. In the case without chromium, the photoresist shows a larger taper than before and the width of the slit has increased to 1.38 and 1.27 µm at the top and bottom of the SiRN, respectively. In both cases, the thickness of the photoresist has been reduced to 1 µm. Figure 3c shows the results after 30 minutes of etching using SF_6. In the case with chromium, some residue of the photoresist can still be seen and the width of the slit has increased to 1.42 and 1.41 µm at the top and bottom of the SiRN, respectively. The chromium layer is still intact, and the surface is smooth. In the case without chromium, there are no resist-residues left and the rough surface shows that the SiRN layer has been etched during processing. Its thickness has decreased from 520 to 357 nm. The width of the slit has increased to 2.16 and 1.61 µm at, respectively, the top and bottom of the SiRN layer.

This shows that the increase in slit width during the etching of the channels is reduced from nearly 90% to less than 25% by using the chromium hard mask. The slit is closed by the conformal LPCVD of SiRN, but will close from the bottom up in the case of a taper as shown in Fig. 3d. This means that the channel might appear closed when testing, but is in fact only closed by a very fragile thin layer. The

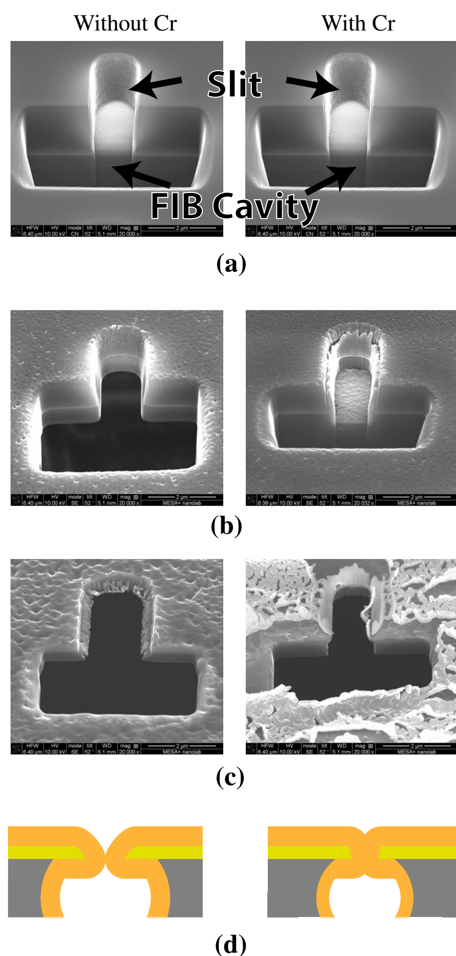

Fig. 3 SEM images of several fabrication steps for etching the channels. The *horizontal rectangular* cavity at the *bottom* is made using focused ion beam etching to obtain a cross section of the *rectangular* slits (in *vertical* direction) with a designed width of 1.2 µm. The *left column* shows the results without a chromium layer resulting in an increase in width by 90%. The *right column* shows the results with a chromium layer, resulting in slits with only slightly increased width. Figure 3a–c corresponds to Fig. 1a in the outline. **a** Slits defined in the photoresist. This is the same with and without chromium. **b** Slits defined in the SiRN layer by directional plasma etching. **c** Channel etched through the slits by (semi-)isotropic etching (30 min). **d** Closed slits after deposition of the final SiRN layer

SEM images shown here show that there will be very little taper when a chromium hardmask is used.

3.2 Silicon etching methods

There are various ways to etch silicon to form the channels through the etch slits (Fig. 1a), release the channels from the bulk or make fluidic access holes to reach the channels from the outside (Fig. 1d). Wet chemical etching can be either isotropic (Schwartz and Robbins 1976) or anisotropic (Bean 1978; Sugiyama et al. 1986; Oosterbroek et al. 2000), resulting in channel cross sections as shown in Fig. 4(1,2). Dry etching can be isotropic using gas-phase etching (Brazzle et al. 2004) or plasma etching (Jansen et al. 1996, 2009), resulting in channel cross sections as shown in Fig. 4(3,4). Dry anisotropic (plasma) etching will result in a cross section as shown in Fig. 4(5) Jansen et al. (1996, 2009).

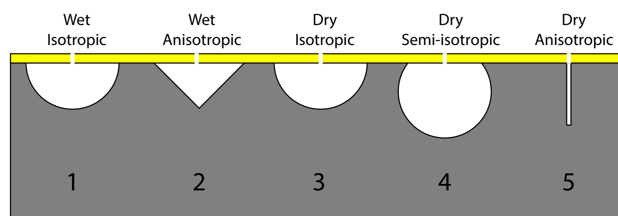

Fig. 4 Cross section of channels etch by different etching methods

A comparison of these methods with respect to their suitability to use them for the channel etch is shown in Table 1. Here, the volumetric etch rate gives a measure for the amount of available etchant for this type of structure and how well it can be controlled. The volumetric etch rate of, for instance, wet chemical isotropic etching with HF/HNO_3 can be very fast. However, the etch rate, and thus the size and shape of the etched channels, is hard to control since it is an auto-catalytic process. The reaction is exothermic and the speed will increase at higher temperatures; some of the reaction products are also etchants by themselves and will thus influence the etch too (Robbins and Schwartz 1959; Schwartz and Robbins 1976).

The shape refers to the shape of the cross section of the channel when etched through a slit, as shown in Fig. 4. Microloading is how much influence size and shape of etch slits/holes have on the etching process and is related to how well the etchant can reach the silicon (and the reaction products can move away). Macro loading is related on how much influence etched structures have to those around and is related to the change in concentration of etchants as a result of etching those structures. The wafer-scale uniformity gives a measure for how uniform the etch rate is over the whole wafer. This is mainly dependent on uniformity in concentration of the etchant at the surface of the wafer and other factors like fluid flow due to temperature gradients or stirring.

SiRN is used as channel material and the top of the channels during etching. The given selectivity to SiRN gives a measure for how much it is attacked during etching.

The surface roughness is a result of disturbed etching of the silicon. In general, a faster etch rate will result in less roughness in the absence of disturbing factors. Usually, microfluidic channels benefit from smooth channel

Table 1 Comparison of etching methods

Typical etchant	Dual source (D)RIE SF_6	Barrel CF_4	Vapour-phase XeF_2	Wet chemical isotropic HF/HNO_3	Wet chemical anisotropic KOH/TMAH
Volumetric etch rate	+	++	++	−	+
Shape (Fig. 4)	4,5	3	3	1	2
Microloading	++	++	++	− −	++
Macro loading	+	−	++	−	++
Uniformity (wafer scale)	+−	− −	++	− −	++
Selectivity to SiRN	+	− −	− −	−	++
Surface roughness	+	++	−	++	++
Reaction products	++	++	−	+	−
Application to:					
Device channel etch	++	++	++	+−	− −
Connection channel etch	++	++	++	+−	−
Release etch	++	−	−	− −	−
Fluidic acces holes	+++	− −	− −	− −	− −

'−' signs indicate negative properties, '+' signs indicate positive properties. In the upper part of the table, properties (taken from literature) of the etch methods are compared. In the bottom part, the applicability to the different etch steps in the process are compared

walls to reduce hydraulic resistance and avoid stiction of particles to the wall.

The reaction products are the results of the chemical reactions taking place during etching and can form a problem for further processing, e.g. KOH etching leaves residue at the etched surface which need to be cleaned before further processing can be done.

Finally, the applicability of the methods for the channel etch and the other silicon etching steps discussed in Groenesteijn et al. (2017) is shown. Of the different methods described, the dry-etching methods are most suited to etch the channels through etch slits. The wet etching methods are unsuited, mainly as a result of the loading effects in wet isotropic etching and the sensitivity to the crystal orientation of wet anisotropic etching. Of the dry-etching methods, using dual source (D)RIE machines (Adixen AMS100 and SPTS Pegasus) has given us the best results. The barrel etcher available to us suffered from non-uniform etch rates and a low selectivity to SiRN. The available vapour-phase XeF_2 etcher has a low selectivity towards SiRN, and the shape and surface roughness depend on the slit pattern. The semi-isotropic dry etching, using SF_6, is sensitive to microloading effects where etching of small features lags behind that of large features; this, however, also gives us several design options when used with etch slits to reach the preferred channel shape and size.

3.3 Channel material

The channel material used to form the channel wall, close the etch slits and form the membrane on top of the etched structures is what determines the channel strength and durability. To support as many applications as possible, there should only be one wetted material in our platform and that material should be chemically inert to many types of fluid. Silicon-nitride (Si_3N_4) and silicon-rich silicon nitride (SiRN, Si_xN_y) are known for their high strength, chemical inertness, stability and good thermal properties (Williams and Muller 1996; Gardeniers et al. 1996; French et al. 1997; Freitag and Richerson 1998; Williams et al. 2003; Kaushik et al. 2005) and can be grown with a conformal step coverage using LPCVD. In addition, it is biocompatible (Mazzocchi and Bellosi 2008), its surface can be functionalized (Parvais et al. 2003; Arafat et al. 2004), and the stress in SiRN can be tuned by the deposition parameters (Gardeniers et al. 1996; Habermehl 1998). The low-stress SiRN we used has a tensile stress of 50–100 MPa compared to silicon. Experience shows that the low intrinsic stress in the SiRN ensures that a relatively thick layer of up to 5 μm can be used and large membranes can be made on top of the channels. The thickness of the initial layer for the slit mask is 500 nm and this leaves a maximum deposition of 2.25 μm, since in the channels it will be deposited on both the top and bottom side of the mask layer. An overview of the relevant properties of SiRN is given in Table 2.

It has been shown that the growth rate of SiRN decreases exponentially inside long channels (Tjerkstra et al. 1997). In our case, this means that after the etch slits are closed, the deposition will be mainly at the fluidic inlets and barely any SiRN will be deposited inside the channels anymore limiting the maximum thickness of the channel wall to half the width of the slits. Since the layer that is then deposited on top of the closed slits is conformal, a small pit remains where the slit used to be, which should be taken

Table 2 Properties of the SiRN films obtained from literature Gardeniers et al. (1996), Habermehl (1998) and measurements

Property	Unit	Value
Extrinsic stress	MPa	50–100 (tensile)
Density	kg m^{-3}	2935.5
Young's modulus	GPa	210
Poisson's ratio	–	0.24

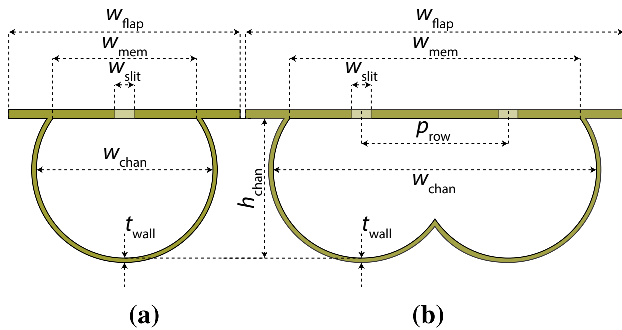

Fig. 5 Schematic overview of a channel made using **a** a single row of slits and **b** two parallel rows of slits

into account when other (functional) layers are placed on top of the channels.

3.4 Empirical channel etch model

Figure 5 gives a schematic overview of the used parameters in the cross section of a channel made by a single row of etch slits ($n_{row} = 1$, Fig. 5a) and by two parallel rows of slits ($n_{row} = 2$, Fig. 5b). Here, the width of the etch slits is denoted by w_{slit}, the width of the channel (w_{chan}) is defined as the widest part of the channel, and the height of the channel (h_{chan}) is the highest/deepest part of the channel. The membrane width (w_{mem}) is the width of the membrane that forms the top of the channel. The flap width (w_{flap}) is the width of the flap on top of the channel after it has been etched free and gives the amount of room available on the channel for transducer structures. This should be chosen larger than w_{mem} to prevent damaging the channel during the etch. The thickness of the wall (t_{wall}) is the thickness of the final SiRN layer. The row pitch (p_{row}) is the distance between two parallel rows of slits. Not shown in the figure are the parameters in length direction of the channels. These are l_{slit} for the length of the slit and p_{slit} for the slit pitch in length direction.

If the etch process is diffusion limited, the volumetric etch rate will be linearly dependent on the area density of etch slits in the Cr/SiRN hard mask. To verify this, 8-mm-long channels were etched with varying width and

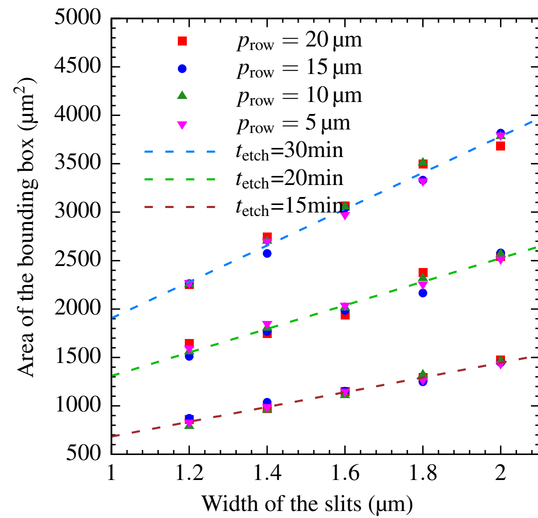

Fig. 6 Cross-sectional area of the etched channels as a function of slit width, slit pitch and etch time. The *dashed lines* are linear regressions of the results with the same etch time

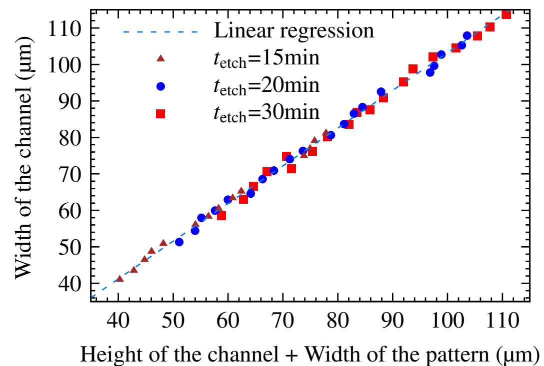

Fig. 7 Width (w_{chan}) vs height + pattern width ($h_{chan} + (n_{row} - 1)p_{row} + w_{slit}$) as a function of etch time. The *dashed line* is a linear regression of all the measurement points

pitch at different etch times. This can be seen in Fig. 6 where a measure for the cross-sectional area is given by the area of a rectangular bounding box around the channel (Area = $h_{chan}w_{chan}$). It can be seen that the etched area is independent of the row pitch, but only dependent on the slit width and etch time. The isotropic process can also be seen when there is a linear relation between the width of the channel (w_{chan}) compared to the width of the slit pattern ($w_{pat} = (n_{row} - 1)p_{row} + w_{slit}$) plus the height of the channel (h_{chan}) as seen in Fig. 7 for the same set of channels as used for Fig. 6. Figure 8 shows SEM images of different channels which are etched using different values of w_{slit} and p_{row}. $n_{row} = 5$ and the etched time (t_{etch}) is, from left to right, 15, 20 and 30 min. It can be clearly seen that for $p_{row} = 10$ μm and $w_{slit} = 1.2$ μm (Fig. 8a), the channel is far wider than its height, while the separate parallel channels only just

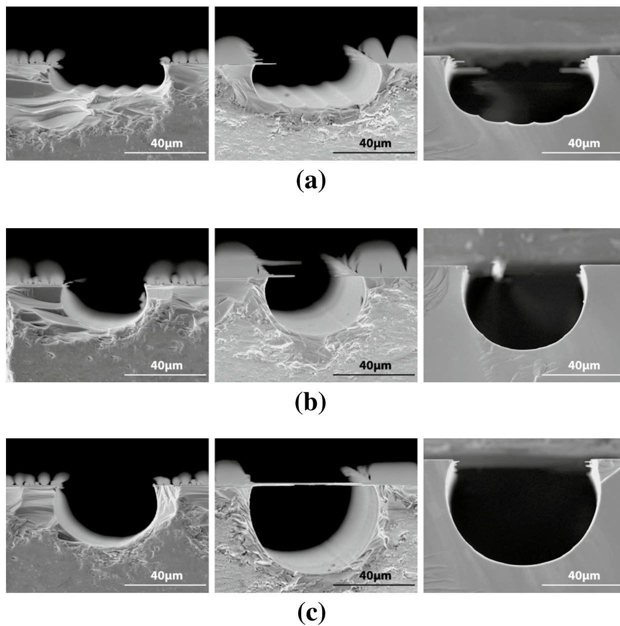

Fig. 8 Various etch results showing the channel shape for five parallel rows of slits. The scale of each image is shown at the *bottom right*. The magnification of all the SEM images is ×1500. **a** $w_{slit} = 1.2\,\mu m$, $p_{row} = 10\,\mu m$, from left to right, t_{etch}= 15, 20 and 30 min. **b** $w_{slit} = 1.2\,\mu m$, $p_{row} = 5\,\mu m$, from left to right, t_{etch}= 15, 20 and 3 min. **c** $w_{slit} = 2\,\mu m$, $p_{row} = 5\,\mu m$, from left to right, t_{etch}=15, 20 and 30 min

reached each other after 15 min of etching. When the etching time increases, the ridges grow smaller and the channel becomes more rounded. For $p_{row} = 5\,\mu m$ and $w_{slit} = 1.2\,\mu m$ (Fig. 8b), the ridges are barely visible after 15 min of etching and the channel becomes larger and rounder when the etch time increases. When the width of the slits is increased to $2\,\mu m$ (Fig. 8c), the ridges are completely gone after 15 min of etching and the channel is significantly larger than with the smaller slit width.

This means that the height, width and shape of the channel can be tuned by tuning the parameters w_{slit}, p_{row} and n_{row} for a certain etch time. To be able to easily find the slit design that will result in the required channel, an empirical model has been made describing the relation between these parameters. Using the parameter variations shown in Table 3, channels have been etched using the Adixen AMS100 dual source (D)RIE machine. Part of the experiment was repeated on an SPTS Pegasus, also at the MESA$^+$ clean room, to measure the influence of the machine on the process. The process settings used in both machines are given in Table 4. The table also specifies the process settings for the directional etch used to etch the SiRN. Since the machines will result in different etch rates, they are compared using a 'base etch rate' (BER). This BER is found by etching a bare silicon wafer using

Table 3 Parameter space used to find the empirical model

Parameter	Unit	Minimum value	Maximum value
n_{row}	–	1	6
p_{row}	μm	5	20
w_{slit}	μm	1.2	2
l_{slit}	μm	5	5
p_{slit}	μm	8	8
t_{etch}	min	5	40

the process settings and by measuring the weight of the wafer before and after the etch, and the amount of etched silicon can be determined. The BER (in $\mu m\,min^{-1}$) is the rate at which the wafer becomes thinner per minute. This gives us an indication of the available amount of etchant that can reach the surface of the wafer. For the process used in the Adixen, this resulted in a BER of $6.07\,\mu m\,min^{-1}$ on a 4-inch wafer, and the process in SPTS resulted in a BER of $16.61\,\mu m\,min^{-1}$ on a 4-inch wafer.

Using the design parameters, a 'slit density' function is defined as:

$$\rho_{slit} = \left(n_{row} - 1\right)\frac{w_{slit}l_{slit}}{p_{row}p_{slit}} + \frac{w_{slit}l_{slit}}{2p_{slit}} \tag{1}$$

The base etch rate is used as a correction on the height of the channel. A surface polynomial as given by Eq. (2) is fitted to the measured height of the channels.

$$h_{fit} = a_0 + \mathrm{BER}\left(p_{00} + p_{10}t_{etch} + p_{01}\rho_{slit} + p_{20}t_{etch}^2 + p_{11}t_{etch}\rho_{slit}\right), \tag{2}$$

where h_{fit} is the fitted height of the channel and t_{etch} is the etch time. The parameter a_0 has been introduced to compensate for starting effects when the channels are not fully formed yet. The fitted width of the channels is then found by using the relation shown in Fig. 7 and fitting a linear correction to the measured width of the channels:

$$w_{fit} = \frac{(n_{row} - 1)p_{row} + w_{slit} + h_{fit} + b_0}{b_1} \tag{3}$$

The resulting fit parameters are found using the curve fitting tool in MATLAB® and are given in Table 5. Figures 9 and 10 show the fitted height and width on the vertical axis, while the measured height and width are shown on the horizontal axis. The points show the different measurement points, and their colour indicates the etch time associated with that measurement. The dashed line indicates an exact match between the measured value and the fitted value. For the height, 88% of the fit results is within ±15% of their measured value, while 95% is within ±15% of their measured width. Here, it should be

Table 4 Process parameters for the dry-etching processes used in the fabrication

Machine profile (Fig. 4)	Unit	Adixen (Fig. 4.4)	SPTS (Fig. 4.4)	Adixen (Fig. 4.5)
Gas: SF_6	sccm	500	600	–
Gas: Ar	sccm	–	–	100
Gas: CHF_3	sccm	–	–	100
Coil power/ ICP	W	2500	3000	1200
Platen power / CCP	W	–	–	150
Process pressure	mbar	0.03	0.1	0.01
Temperature	°C	20	−19	20
Base etch rate	µm min^{-1}	6.07	16.61	–

Table 5 Fit parameters found using the curve fitting tool in MATLAB®

Parameter	Value	Parameter	Value
a_0	−4.056 µm	p_{00}	0.027543 min
p_{10}	0.11679	p_{01}	0.82039 min
p_{20}	−0.0012005 min^{-1}	p_{11}	0.11973
b_0	−1.5482 µm	b_1	0.94423

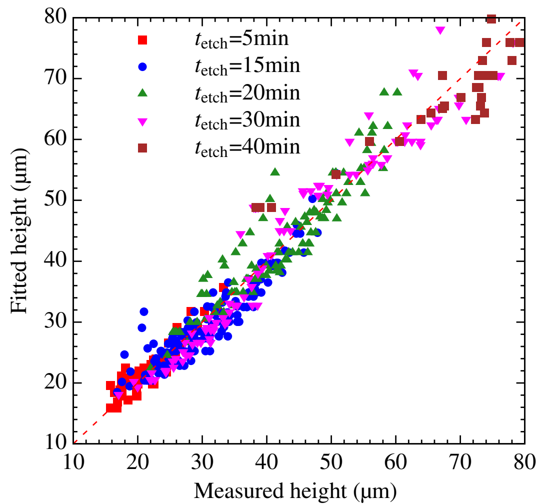

Fig. 9 Fitted height versus measured height of the channels etched using the design parameters given in Table 3

noted that only channels are taken into account where the channels are etched far enough that the parallel rows of slits result in a single channel without significant ridges between them, ie. $p_{row} << h_{measured}$.

3.5 Channel design using the model

These results show that the eventual height and width of the channel can be found when all design parameters are known. However, to be useful, we want to know the slit pattern that is required for channels of a desired height and width. Of the design parameters given earlier in this section (w_{slit}, p_{row}, n_{row} and t_{etch}), w_{slit} is least suitable to change per design, since it is also related to the wall thickness. The etch time determines the minimum channel height of a single row of slits and cannot be determined per design, but only for the whole wafer. As a result, only the amount of parallel slits (n_{row}) and the distance between these rows (p_{row}) can be optimized for specific channel shapes. This can be done by rewriting (Eq. 3) for p_{row} as a function of n_{row} and the desired height and width:

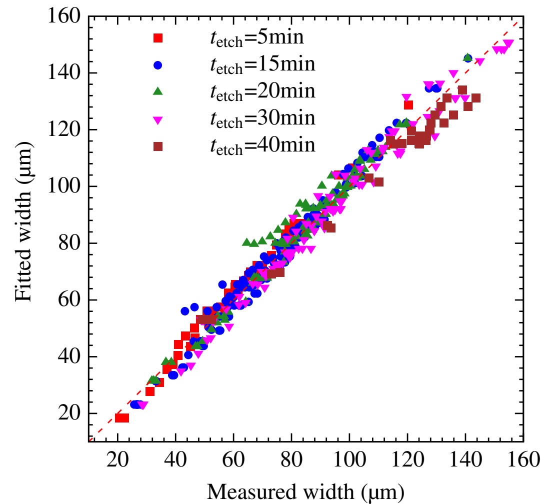

Fig. 10 Fitted width versus measured width of the channels etched using the design parameters given in Table 3

$$p_{row} = \frac{w_{desired} b_1 - w_{slit} - h_{desired} - b_0}{n_{row} - 1} \quad (4)$$

where n_{row} can be found by equating Eqs. (2) and (3) to the desired height and width and using a minimum error algorithm, while keeping in mind that n_{row} can only have integer values. An example of this is shown graphically in Fig. 11, where a least-square approximation according to

$$\sqrt{(h_{fit} - h_{desired})^2 + (w_{fit} - w_{desired})^2}, \quad (5)$$

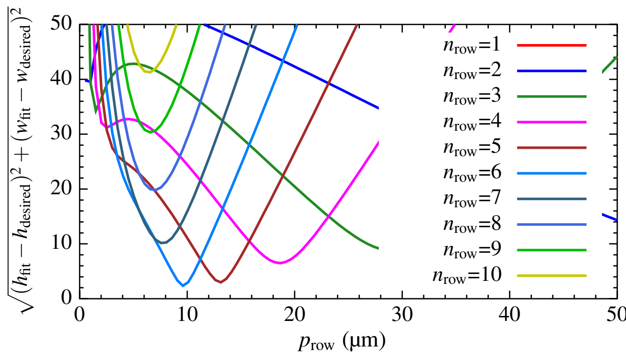

Fig. 11 The least-square error plotted for various values of n_{row}, with p_{row} in the range of 0 to 50 µm and $h_{desired}$ = 30 µm, $w_{desired}$ = 85 µm and an etch time of 20 min with the Adixen etcher

is plotted for various values of n_{row} and p_{row} in a range of 0–50 µm. The desired height $h_{desired}$ and width $w_{desired}$ are 30 and 85 µm, respectively. The chosen etch time is 20 min with the Adixen etcher. The graph shows a minimum error for n_{row} = 6, using this value in Eq. (4) results in a pitch of p_{row} = 9.96 µm and, from Eqs. (2) and (3), a height and width of 31.8 and 86.9 µm, respectively.

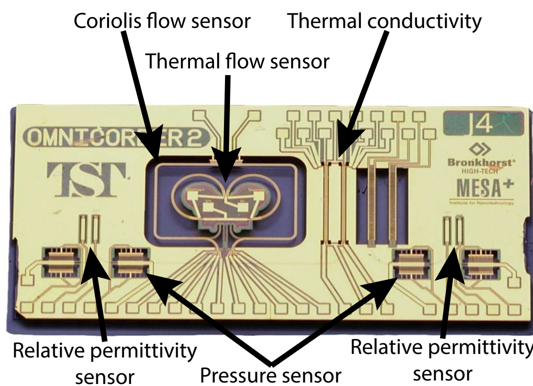

Fig. 12 Photograph of the single-chip multi-parameter microfluidic measurement system. The locations of the separate sensors are indicated

4 Example channel designs for a multi-parameter flow sensor

In Lötters et al. (2014, 2015), Groenesteijn (2016) we proposed a single-chip multi-parameter microfluidic measurement system made in the fabrication process outlined in Sect. 2. The system comprises a thermal flow sensor, a Coriolis flow and density sensor, a relative permittivity sensor, pressure sensors (both at the inlet and outlet) and a thermal conductivity sensor. Using these sensors, the composition of mixtures can be calculated from the physical properties density, viscosity, heat capacity, thermal conductivity and relative permittivity. A photograph of the final chip is shown in Fig. 12. An overview of the different channels is shown in Table 6, while SEM images of their cross sections are shown in Fig. 13. Each of the sensors poses different requirements on the size and shape of the channel.

4.1 Flow sensors

The fluid flow is measured using two methods: using a thermal (calorimetric) flow sensor and using a Coriolis flow sensor. In Groenesteijn (2016), Groenesteijn et al. (2016), it was shown that, to have an overlapping flow range, the Coriolis channel should have a small diameter, while the thermal sensor should very long. To keep the pressure drop low, this means the diameter should be large. Of all the sensors on the chip, the Coriolis channel has the most benefit of a small diameter and the desired width (45 µm) thus dictates the minimum channel size for n_{slit} = 1. According to the model shown in Sect. 3.4, this would require an etch time of 15 min when slits of 1.5 µm are used and the channels are etched using the SPTS machine. At a heater length of 1750 µm, the channel of the thermal flow sensor should not cause too much pressure drop and should thus be relatively large. For this, a channel width of about 30% larger than that of the Coriolis channel (= 60 µm) is chosen. Since the channel needs to be etched completely free, it should not be much higher than the Coriolis channel. Using

Table 6 Overview of the measured and predicted sizes of the channels used in the shown examples

Device	Figure	n_{row}	p_{row} (µm)	Measured width (µm)	Modelled width (µm)	Error %	Measured height (µm)	Modelled height (µm)	Error (%)
Coriolis flow sensor	13a	1	–	42.9	44	2.0	35.2	41	14.9
Thermal flow sensor	13b	2	10	64.3	59	−9.6	47.5	45	−4.5
Relative permittivity	13c	3	29	104.3	108	3.6	41.3	44	6.6
Pressure sensor	13d	4	10	94	89	−6.5	61	54	−13.8
Thermal conductivity	13e	1	–	43.5	44	0.7	35.5	41	14.2

SEM images of cross sections of the channels are shown in Fig. 13

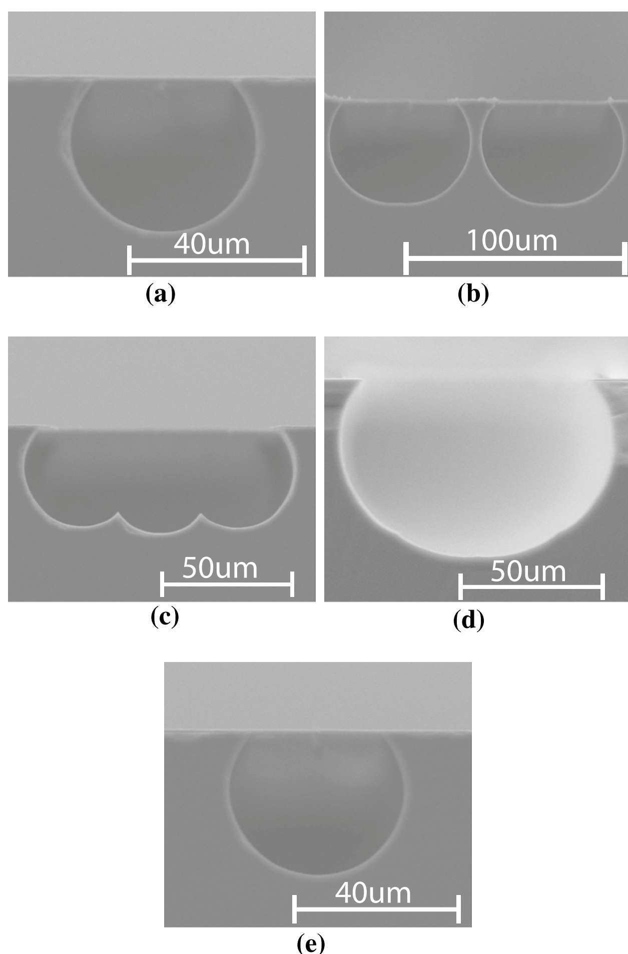

Fig. 13 SEM images of the channel shapes and sizes used for the different devices in the multi-parameter flow sensor. **a** Coriolis mass flow sensor. **b** Thermal flow sensor. **c** Relative permittivity sensor. **d** Pressure sensor. **e** Thermal conductivity sensor

$n_{\mathrm{slit}} = 2$ and $p_{\mathrm{slit}} = 10$. To fully release both channels from the bulk of the chip, release holes of at least 250 µm are etched on each side of the channels. For each sensor, the modelled and measured channel dimensions are shown in Table 6.

4.2 Relative permittivity sensor

The relative permittivity of a fluid can be measured by measuring the (parallel plate) capacitance between an electrode on top of the channel and the grounded substrate underneath the channel. The capacitance C is then dependent on the area of the electrode (length and width of the channel), the distance between the electrodes (height of the channel) and the relative permittivity of the fluid. Using a channel of 110 µm wide, 700 µm long and 45 µm deep, the resulting capacitance when the channel is filled with air ($\varepsilon_r = 1$) is 15 fF. Filled with water ($\varepsilon_r = 80$), this would increase to 1.2 pF. These dimensions can be achieved by using $n_{\mathrm{slit}} = 3$ and $p_{\mathrm{slit}} = 29$.

4.3 Pressure sensor

The deformation of a channel depends on the pressure inside the channel and can be measured by measuring the tilt of the membrane on top of the channel using capacitive comb structures. While a wide membrane will result in a large tilt, it also reduces the maximum pressure. A membrane of 90 µm wide will be able to withstand a pressure up to 2 bar (Alveringh et al. 2015) and can be made using $n_{\mathrm{slit}} = 4$ and $p_{\mathrm{slit}} = 10$. Due to the relatively large channel, the pressure drop over the pressure sensor will be low compared to that of the rest of the chip and the measured value will be the average pressure inside the whole pressure sensor.

4.4 Thermal conductivity sensor

The thermal conductivity of the fluid can be measured by measuring how much heat leaks away through the fluid to the silicon bulk. To reduce the influence of the fluid flow and conduction through the channel wall, the channel should be long and have a small diameter. In this case, that means the same dimensions as the channel of the Coriolis sensor. The channel, shown in Fig. 13e, is the same design as that of the Coriolis sensor.

5 Discussion

As shown in the previous section, using the proposed microfluidic platform gives a lot of design freedom to make the required channel for a wide variety of devices. However, there are some limits that might mean this platform is not suitable for a certain application. Some of the limitations might be circumvented by adding additional fabrication steps. The channels will, for instance, always have a semi-circular shape due to the semi-isotropic etch process used to etch them. However, usage of a silicon-on-insulator wafer with a buried oxide layer already showed that the bottom of the channel can be made very flat. Straight side walls could by created by etching trenches and filling them with SiRN before the channel etch and together they can be used to make rectangular channels.

A method is presented to predict the size and shape of the etched channels, based on the amount of parallel slits and the spacing between them. This method is based on an empirical model, and the validity outside the used design parameters is hard to predict. In particular, the used etch time has a large influence on the validity of the model

due to the square in Eq. (2). While nearly all the results fit within ±15% of their measured value, the ones that do not are mainly with long etching time. It has shown to be easily adaptable to the two different etching machines that are available to us by introducing a base etch rate. Adapting the model to different etching machines should thus be relatively easy, provided the shape of the cross section of the etched channel is similar to the one shown in Fig. 4(4).

The results in Figs. 9 and 10 and Table 6 show that the measured dimensions of the channel can vary from the modelled dimensions. This is a result of several factors that have not been included in the model. One of the main reasons is the uniformity of used etching machine. As shown in Donnelly and Kornblit (2013), Lee et al. (2014), etching with a plasma etcher is a balance between chemical and physical etching. The etch rate of each of these components is depending on for instance plasma uniformity, concentration of the etchant and charging of the wafer. As a result, the uniformity of the two dry-etching steps that determine the channel shape and size (directional etch of the slits through the SiRN layer and semi-isotropic etch of the silicon underneath the SiRN layer) has a large influence on the final channel. Additionally, the slits are patterned using contact lithography with relatively thick photoresist (1.7 µm). This thickness is required for the two etching steps and limit the accuracy of mainly the width of slits. Together, these two effects can cause a non-uniformity in the channel size over the wafer. Due to the complexity of the interaction of these effects, they have not been included in the model. However, they can be reduced by improving the control over etching and lithography process (i.e. further tuning the etching recipes, using more uniform etching machines or thinner resist).

6 Conclusions

In this paper, a method to design and fabricate microfluidic channels in a wide range of sizes and shapes on the same chip has been presented. General design rules and limitations are given to help to design the required channel for a specific application. By being able to fabricate channels with diameters from less than 10 µm to well over 100 µm in close proximity to each other, a wide variety of microfluidic devices can be integrated on the same chip with little dead volume between them. An empirical model is presented to determine the required slit pattern for channels of a desired size and shape. The presented model can predict the resulting channel within 15% of the measured dimensions. To further improve the model, the uniformity of the used plasma etch machines will have to be studied. Together with the functionalization options presented in part 1 of this paper, this gives a versatile microfluidic fabrication platform that allows for integration of many different microfluidic devices on the same chip.

Several examples are given of devices made using this platform to show how the model can be used to integrate these devices on the same chip.

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