Circuits Syst Signal Process (2013) 32:433–451
DOI 10.1007/s00034-012-9469-z

A Very Fast Method for the DC Analysis of Diode–Transistor Circuits

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Received: 14 February 2012 / Revised: 21 July 2012 / Published online: 8 August 2012

Abstract The paper offers a universal method for finding a unique or multiple DC operating points of nonlinear circuits. The developed method is based on the theory known as a linear complementarity problem (LCP) and the homotopy concept. It is a combination of Lemke's method for solving LCP and some variant of the homotopy method. To express the problem of finding DC operating points in terms of LCP, an appropriate piecewise–linear approximation of diode characteristic is proposed. Although the method does not guarantee finding all the DC operating points, usually it finds them. The method is very fast and remarkably efficient. Numerical examples, including practical BJT and CMOS circuits having a unique or multiple DC operating points are given.

Keywords DC analysis · Homotopy method · Linear complementarity problem · Transistor circuits

1 Introduction

The basic question of the analysis of nonlinear electronic circuits is finding DC operating points (DC solutions) [2, 23]. The circuits having a unique operating point are usually analyzed using the Newton–Raphson method [2, 10]. Unfortunately, the method may be divergent or oscillating if the initial guess is not sufficiently close to the solution. Even if the method gives the solution, the rate of convergence may be low, in particular for large sized circuits. The Newton–Raphson method is employed

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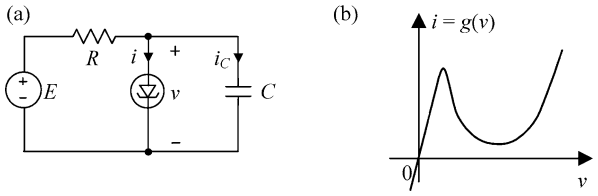


Fig. 1 A nonlinear dynamic circuit (**a**) and the v–i characteristic of the tunnel diode (**b**)

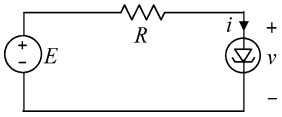


Fig. 2 Resistive circuit obtained from the circuit shown in Fig. 1 after removing the capacitor C

in the SPICE simulator [8, 12], where different concepts and techniques have been implemented in order to overcome the convergence problems. These modifications improve the convergence but make the method complex and consuming more CPU time.

A broad class of electronic circuits has multiple DC operating points. To explain when and how they exist, we consider a nonlinear dynamic circuit shown in Fig. 1a, including a tunnel diode, specified by the characteristic depicted in Fig. 1b. The circuit can be described by the differential equation

$$\frac{\mathrm{d}v}{\mathrm{d}t} = \frac{1}{C}\left(\frac{E-v}{R} - g(v)\right). \tag{1}$$

To find the equilibrium points of the circuit, we set to zero $\mathrm{d}v/\mathrm{d}t$ (remove the capacitor), obtaining the algebraic equation

$$g(v) = \frac{E}{R} - \frac{v}{R}. \tag{2}$$

Equation (2) describes the nonlinear resistive circuit shown in Fig. 2. To solve this equation, we apply the graphical method illustrated in Fig. 3. As a result, we find three solutions v^*, v^{**}, v^{***}, corresponding to the intersection points A, B, C. The obtained solutions are called DC operating points or DC solutions. The three solutions occur for certain values of E and R. Figure 3 shows that for larger value $\tilde{E}$ of the voltage source the circuit has a unique DC operating point $\tilde{v}^*$ corresponding to the intersection point D. Thus, the existence of multiple DC operating points depends on the circuit topology, circuit elements and values of the sources.

The DC operating points can be considered as the equilibrium points of the dynamic circuit shown in Fig. 1a. The equilibrium points of a dynamic circuit can be stable or unstable in Lapunov's sense. Having the equilibrium points (the DC operating points), we can next apply to each of them an appropriate method based on Lapunov's concept, e.g. [16, 17] to separate them into stable (asymptotically stable) and unstable. In the exemplary circuit shown in Fig. 1, the equilibrium points v^* and v^{***} are asymptotically stable, whereas v^{**} is unstable. The question which of the solutions v^*, v^{***} actually occurs depends on initial conditions in the dynamic circuit (see Fig. 1).

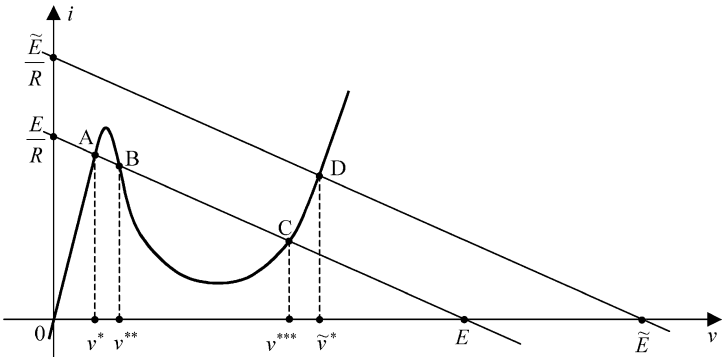


Fig. 3 Illustration of a graphical method for finding the DC solutions

Finding multiple DC operating points is an even more difficult task in circuit simulation. Several methods have been recently proposed for solving this problem, e.g. [4, 6, 9, 11, 13, 15, 19–22, 24, 25]. Not all the methods developed in the above mentioned references determine all the DC operating points. The methods that guarantee finding all the DC operating points are very time consuming and are capable to analyze only small size circuits. Many commonly used methods in this area are based on piecewise–linear approximations and computation techniques, e.g. [11, 15, 19, 24, 25].

Thus, different methods and computation techniques can be used depending on whether the analyzed circuit has a unique or multiple DC operating points. Unfortunately, this question is usually not known in advance and a universal method is usually required, enabling us to efficiently perform the DC analysis in any case.

Numerous papers devoted to the DC analysis of nonlinear circuits have employed different variants of the homotopy method, also known as the continuation method, e.g. [7, 9, 18, 24]. The method deforms the equations describing the circuit by embedding a parameter λ that varies tracing a solution path. Each intersection of this path with $\lambda = 1$ plane is a solution of the equations. The homotopy method is a powerful tool for finding a unique or multiple DC operating points.

Another interesting approach to the analysis of nonlinear DC circuits is based on the theory known as a linear complementarity problem (LCP) [3, 5]. To find DC operating points, the circuit is described in the form of LCP and solved using Lemke's method. References [15, 25] show some applications of this approach to the DC analysis of different classes of nonlinear circuits.

In this paper, the problem of finding a unique or multiple DC operating points of BJT and CMOS circuits is expressed in terms of LCP and solved using an algorithm being a combination of Lemke's method and some variant of the homotopy method [3, 5]. The algorithm is easy for computer implementation, very fast and remarkably efficient. This approach is entirely different than the method proposed in [22], for finding multiple DC operating points, being a combination of deflation technique, enabling us to avoid the solutions earlier determined, with some variant of the Newton–Raphson nodal analysis.

Consider a circuit consisting of bipolar transistors, diodes, resistors and voltage sources. The transistors are characterized by the Ebers–Moll model composed of two

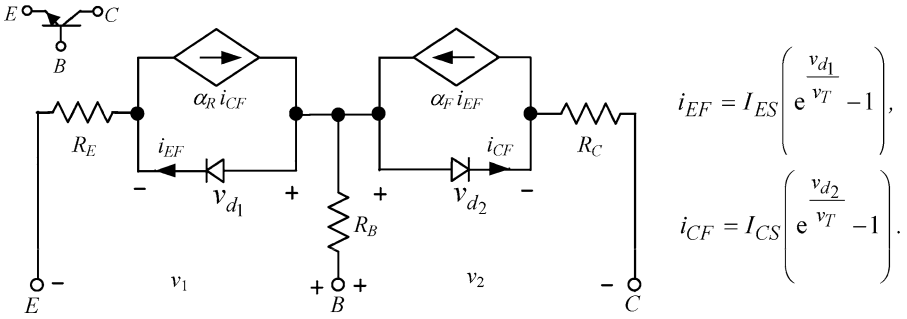
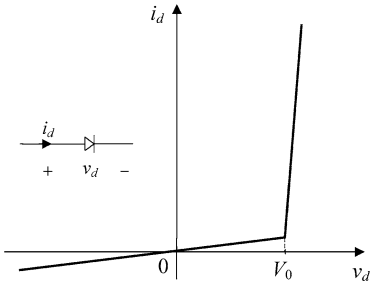


Fig. 4 Ebers–Moll model for a npn transistor

Fig. 5 A piecewise–linear diode characteristic



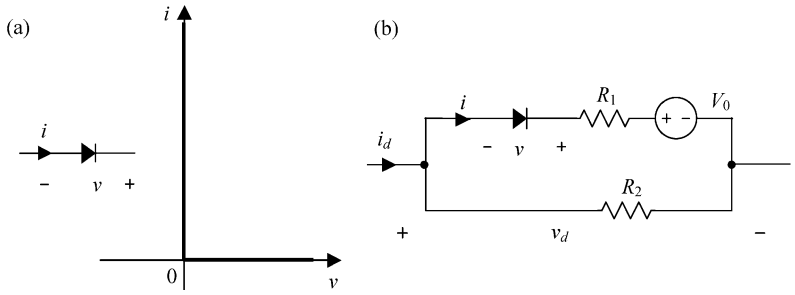


Fig. 6 Ideal diode characteristic (**a**) and a model of the diode having the characteristic shown in Fig. 5(**b**)

diode–controlled source combinations and the emitter, base, and collector resistors [2] (see Fig. 4). A simple two-segment piecewise-linear characteristic of each diode included in the Ebers–Moll model or acting alone is shown in Fig. 5.

The characteristic is synthesized using an ideal diode, having the characteristic shown in Fig. 6a, a voltage source and two resistors as depicted in Fig. 6b. Note that the reference direction of the voltage v across the ideal diode in Fig. 6 is different than the reference direction of the voltage v_d (see Fig. 5).

A more accurate characteristic of a diode consists of three (or generally m) linear segments (see Fig. 7a). It can be synthesized by the circuit shown in Fig. 7b.

To describe the circuit, we replace all the diodes by the model shown in Figs. 6b or 7b and extract the ideal diodes from the circuit. As a result an n-port is created,

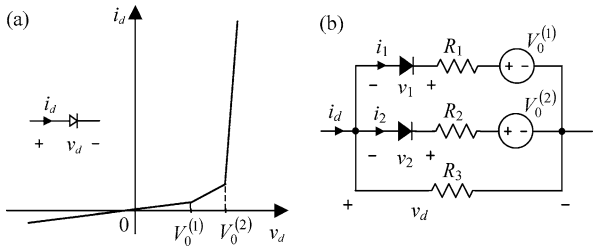


Fig. 7 Three-segment characteristic of a diode (**a**) and its model (**b**)

consisting of resistors, independent voltage sources and current–controlled current sources (see Fig. 8). Using the admittance representation of the n-port, we write

$$\boldsymbol{i} = \boldsymbol{G}\boldsymbol{v} + \boldsymbol{b}, \tag{3}$$

where $\boldsymbol{i} = [i_1 \cdots i_n]^{\mathrm{T}}$, $\boldsymbol{v} = [v_1 \cdots v_n]^{\mathrm{T}}$ are vectors of the port currents and voltages, $\boldsymbol{b} = [b_1 \cdots b_n]^{\mathrm{T}}$ is a source vector, $\boldsymbol{G} = [g_{ij}]_{n\times n}$ is the short-circuit admittance matrix. The reference directions of the port voltages and currents are as shown in Fig. 8. Then, the ideal diodes terminating the n-port are described as follows:

$$i_j \geq 0, \qquad v_j \geq 0, \qquad i_j v_j = 0, \quad j = 1, \ldots, n. \tag{4}$$

Thus, the circuit depicted in Fig. 8 has the description

$$\begin{aligned} &\boldsymbol{i} = \boldsymbol{G}\boldsymbol{v} + \boldsymbol{b}, \\ &\boldsymbol{v} \geq \boldsymbol{0}, \ \boldsymbol{i} \geq \boldsymbol{0}, \quad \boldsymbol{i}^{\mathrm{T}}\boldsymbol{v} = 0. \end{aligned} \tag{5}$$

The problem specified by (5) is called a linear complementarity problem (LCP) [3, 5]. To formulate this problem in a standard form we denote: $\boldsymbol{i} = \boldsymbol{z} = [z_1 \cdots z_n]^{\mathrm{T}}$, $\boldsymbol{v} = \boldsymbol{x} = [x_1 \cdots x_n]^{\mathrm{T}}$, $\boldsymbol{b} = \boldsymbol{q} = [q_1 \cdots q_n]^{\mathrm{T}}$, $\boldsymbol{G} = \boldsymbol{M} = [m_{ij}]_{n\times n}$. Then the LCP is stated as follows.

Find a vector $\boldsymbol{x} \in R^n$ such that for

$$\boldsymbol{z} = \boldsymbol{q} + \boldsymbol{M}\boldsymbol{x} \tag{6}$$

we have

$$\boldsymbol{x} \geq \boldsymbol{0}, \ \boldsymbol{z} \geq \boldsymbol{0}, \quad \boldsymbol{z}^{\mathrm{T}}\boldsymbol{x} = 0.$$

We term x_i the complement of z_i and vice versa ($i = 1, \ldots, n$).

2 Finding Multiple DC Operating Points Using LCP

To solve the linear complementarity problem, we apply the homotopy approach combined with Lemke's algorithm [3, 5] as described in the sequel.

First we chose a positive vector $\boldsymbol{d} = [d_1 \cdots d_n]^{\mathrm{T}} \in R^n$ such that $\boldsymbol{d} + \boldsymbol{q} > \boldsymbol{0}$ and define the homotopy

$$\boldsymbol{z}^{\mathrm{T}}\boldsymbol{x} = 0, \quad \boldsymbol{x} \geq \boldsymbol{0}, \ \boldsymbol{z} \geq \boldsymbol{0},$$

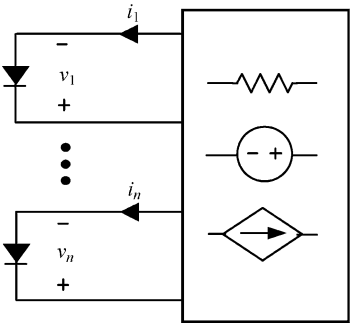


Fig. 8 The circuit with extracted ideal diodes

$$z = p - \lambda d + Mx, \tag{7}$$

where $p = [p_1 \cdots p_n]^{\mathrm{T}} = (d + q) > 0$ and λ is a real variable. At $\lambda = 0$ equation (7) reduces to $z = p + Mx$ and the solution $x = 0$ of the homotopy system is obtained. At $\lambda = 1$ we have the original LCP (6).

To create vector d the following heuristic procedure is applied. Find the minimal value q^- , the maximum value q^+ of the set $\{q_1, \ldots, q_n\}$ and the mean value s of $\{|q_1|, \ldots, |q_n|\}$. Next form the interval $[d^-, d^+]$, where

$$d^- = \begin{cases} 0.05s - q^- & \text{if } q^- < 0, \\ 0.05s & \text{if } q^- \geq 0, \end{cases} \qquad d^+ = \begin{cases} 1.1q^+ & \text{if } q^+ > d^-, \\ 1.1(d^- + s) & \text{if } q^+ \leq d^-. \end{cases}$$

Components $d_i (i = 1, \ldots, n)$ of the vector d are obtained by random selection from the interval $[d^-, d^+]$, assuming uniform distribution.

To trace the homotopy path, we apply the concept of Lemke's algorithm [3, 5]. According to this algorithm, we designate either x_i or z_i to be zero for each i throughout any step. At each step there are $n + 1$ zero variables, i.e. for some i both $x_i = 0$ and $z_i = 0$. One of these variables, called a distinguished variable, is increased by adjusting another variables and λ.

2.1 Sketch of the Algorithm

We start from the solution $x = 0$ of the homotopy system corresponding to $\lambda = 0$ and substitute it into (7)

$$z = p - \lambda d, \tag{8}$$

where $p > 0, d > 0$ and for $\lambda = 0, z = p$. Then we find

$$\lambda^{(1)} = \min\left\{\frac{p_i}{d_i}\right\}, \quad i = 1, \ldots, n.$$

Assume that a week condition called a regularity condition [5] is satisfied: for all solutions (x, λ) to the homotopy system at least $n - 1$ of the variables x, z are greater than zero. If $\lambda^{(1)}$ corresponds to $i = l$, we obtain the point of minimum, such that $z_l = 0$ and $z_i > 0$ for $i = 1, \ldots, l - 1, l + 1, \ldots, n$. Let us take into account lth scalar

equation of (7), solve it for x_l (the complement of z_l) and substitute into the other scalar equations of (7). As a result we have

$$\begin{aligned} x_l &= \frac{d_l}{m_{ll}}\lambda - \frac{p_l}{m_{ll}} + \frac{z_l}{m_{ll}} - \sum_{j=1,j\neq l}^{n} \frac{m_{lj}}{m_{ll}} x_j, \\ z_i &= \left(-d_i + \frac{m_{il}}{m_{ll}} d_l\right)\lambda + \left(p_i - \frac{m_{il}}{m_{ll}} p_l\right) + \frac{m_{il}}{m_{ll}} z_l \\ &\quad + \sum_{j=1,j\neq l}^{n} \left(m_{ij} - \frac{m_{ij}m_{lj}}{m_{ll}}\right) x_j, \quad i = 1,\ldots,l-1,l+1,\ldots,n. \end{aligned} \tag{9}$$

The set of (9) is equivalent to (7) and for $\lambda = \lambda^{(1)}$ has the solution: $x_i = 0, i = 1,\ldots,n$, with $z_l = 0$, and $z_i > 0$ for $i = 1,\ldots,l-1,l+1,\ldots,n$. Thus, $(\boldsymbol{x} = \boldsymbol{0}, \lambda = \lambda^{(1)})$ is a break-point of the homotopy path. Substituting $z_l = 0, x_j = 0, j = 1,\ldots,l-1,l+1,\ldots,n$ into (9) yields

$$x_l = \frac{d_l}{m_{ll}}\lambda - \frac{p_l}{m_{ll}}, \tag{10}$$

$$z_i = \left(-d_i + \frac{m_{il}}{m_{ll}} d_l\right)\lambda + \left(p_i - \frac{m_{il}}{m_{ll}} p_l\right), \quad i = 1,\ldots,l-1,l+1,\ldots,n. \tag{11}$$

We eliminate λ from (11) using (10), obtaining after simple manipulations

$$z_i = \left(p_i - \frac{d_i}{d_l} p_l\right) + \left(m_{il} - \frac{d_i}{d_l} m_{ll}\right) x_l, \quad i = 1,\ldots,l-1,l+1,\ldots,n, \tag{12}$$

where $z_i > 0$ for $x_l = 0$. Now x_l is increased from zero and suppose that for some positive value of x_l a variable z_i becomes zero. To find this variable, a set J of the subscripts i is formed so that

$$m_{il} - \frac{d_i}{d_l} m_{ll} < 0. \tag{13}$$

Next we find

$$x_l = \min_{i\in J} \left\{ -\frac{p_i - \frac{d_i}{d_l} p_l}{m_{il} - \frac{d_i}{d_l} m_{ll}} \right\} > 0, \tag{14}$$

and choose the subscript i corresponding to the minimum, say $i = k$. Then $z_k = 0$ and its complement x_k becomes the new distinguished variable which is to be increased. Using (10) we find the new value of λ

$$\lambda^{(2)} = \frac{p_l}{d_l} + \frac{m_{ll}}{d_l} x_l. \tag{15}$$

Thus, $\boldsymbol{x} = [0\cdots 0\, x_l\, 0\cdots 0]^{\mathrm{T}}$ and $\lambda^{(2)}$ form a subsequent break-point of the homotopy path. We continue the described approach, taking into account the new distinguished

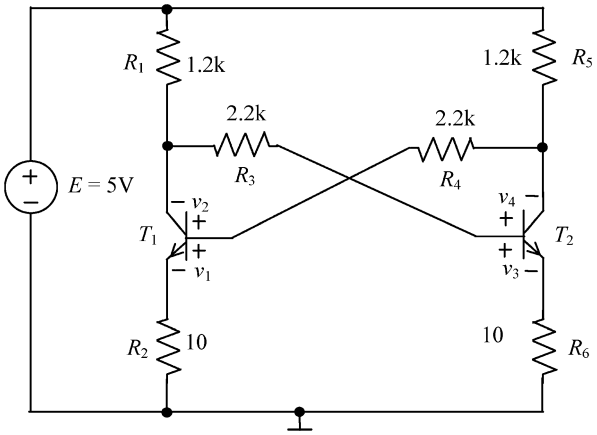


Fig. 9 Circuit for Example 1

variable. The values of $\lambda^{(i)}$ and the corresponding solutions form break-points of a homotopy path. When the path intersects $\lambda = 1$ plane, then the solution corresponding to $\lambda = 1$ is the solution of the original LCP (6).

If the circuit has a unique DC operating point, the tracing of the homotopy path is carried out until it crosses the $\lambda = 1$ plane. This point determines the solution. If the circuit has multiple DC operating points, however, the above described algorithm should be continued as long as it is possible, allowing to increase or decrease λ, to find other intersection points of the homotopy path with the $\lambda = 1$ plane. Each of these points leads to a solution. The approach is visualized in Example 1 (Figs. 10, 11), where the algorithm gives three DC operating points.

If the algorithm fails at some stage of the procedure, it is terminated and started again using a different vector d obtained by random selection of its components from the interval $[d^-, d^+]$, according to the procedure developed in this section.

3 Numerical Examples

The proposed method was implemented in MATLAB 2009b and tested using several circuits. The calculations were executed on a computer with the processor Intel (R) Core (TM) i7 Q820@1.73 GHz.

3.1 Example 1

To explain in detail the method proposed in Sect. 2, we consider a very simple BJT circuit shown in Fig. 9. The transistors are characterized by the Ebers–Moll model (Fig. 4) having the following parameters: $\alpha_F = 0.99, \alpha_R = 0.5$, $I_{ES} = 7.139$ fA, $I_{CS} = 14.136$ fA, $V_T = 25.86$ mV, $R_E = R_C = 10\ \Omega$, $R_B = 3\ \Omega$.

To find the DC operating points of this circuit, we apply the method developed in Sect. 2. For this purpose the emitter and collector diodes are modeled by the circuit shown in Fig. 7b, with the following parameters:

Emitter diode

$$R_1 = 28.88\ \Omega, \qquad R_2 = 5.192\ \Omega, \qquad R_3 = 1\ \text{G}\Omega, \qquad V_0^{(1)} = 0.630\ \text{V},$$

$$V_0^{(2)} = 0.688 \text{ V},$$

Collector diode

$$R_1 = 24.547\ \Omega, \qquad R_2 = 5.498\ \Omega, \qquad R_3 = 1\ \text{G}\Omega, \qquad V_0^{(1)} = 0.620 \text{ V},$$

$$V_0^{(2)} = 0.669 \text{ V}.$$

At first the representation (3) of the circuit is created using a computer program written in Delphi. Next, the vector $\boldsymbol{d}$ is generated by the procedure described in Sect. 2 and the homotopy (7) is formulated. The method starts from $\boldsymbol{x} = \boldsymbol{0}, \lambda = 0$ and traces the homotopy path that intersects the $\lambda = 1$ plane at three points, corresponding to three DC operating points, leading for each of the points to voltages and currents of the ideal diodes. They enable us to find voltages across the piecewise-linear diodes, modeled by the circuit shown in Fig. 7b, and next, voltages across the resistors R_E, R_C, and R_B of the transistors. As a result we obtain the BE and BC voltages.

As a result we find

$$\tilde{\boldsymbol{v}}^* = \begin{bmatrix} 0.763 \\ 0.634 \\ 0.181 \\ -3.342 \end{bmatrix}, \qquad \tilde{\boldsymbol{v}}^{**} = \begin{bmatrix} 0.729 \\ -0.075 \\ 0.729 \\ -0.075 \end{bmatrix}, \qquad \tilde{\boldsymbol{v}}^{***} = \begin{bmatrix} 0.181 \\ -3.342 \\ 0.763 \\ 0.634 \end{bmatrix}, \tag{16}$$

where the elements of these vectors correspond to the voltages v_1, v_2, v_3, and v_4, in volts, indicated in Fig. 9.

Figure 10 shows the projection of the obtained homotopy path on the plane $\lambda - x_3$, where x_3 is the voltage across the ideal diode included in the model of the collector diode of the transistor T_1. The plots of λ and x_3 against the numbers of the computation steps are shown in Fig. 11.

The obtained operating points are approximate, due to piecewise-linear representations of the diodes. Therefore, next we use each of them in succession as the initial guess in the Newton–Raphson method. Performing only two iterations in each case, we obtain the corrected operating points listed below:

$$\boldsymbol{v}^* = \begin{bmatrix} 0.767 \\ 0.631 \\ 0.188 \\ -3.336 \end{bmatrix}, \qquad \boldsymbol{v}^{**} = \begin{bmatrix} 0.730 \\ -0.075 \\ 0.730 \\ -0.075 \end{bmatrix}, \qquad \boldsymbol{v}^{***} = \begin{bmatrix} 0.188 \\ -3.336 \\ 0.767 \\ 0.631 \end{bmatrix}. \tag{17}$$

They are very close to the solutions (16). Also the SPICE (ICAP/4) simulator gives the same operating points, starting in succession from each of the obtained solutions (16), rearranged into node voltages. In the SPICE simulations the Gummel–Poon model of the transistors is employed with the parameters corresponding to the parameters of the Ebers–Moll model described in this example. In particular, the same resistors R_E, R_C, and R_B are included and the voltages $v_1, \ldots, v_4$ consist of the junction voltages and the voltages across the corresponding resistors (see Fig. 4). Identical results are obtained applying the exhaustive method which guarantees finding all DC operating points [20].

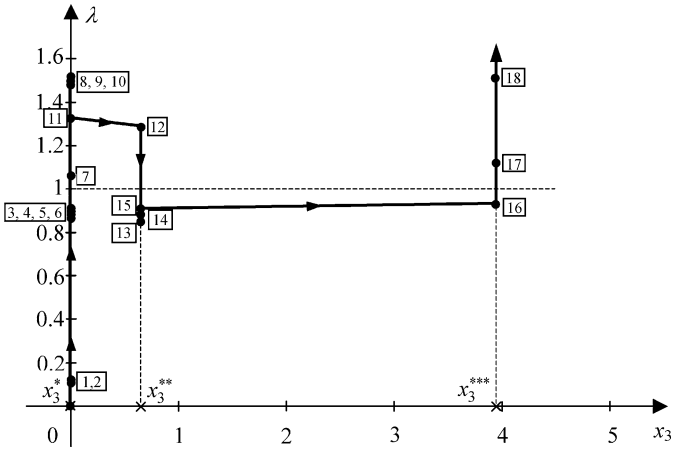


Fig. 10 Projection of the homotopy path on the plane λ–x_3

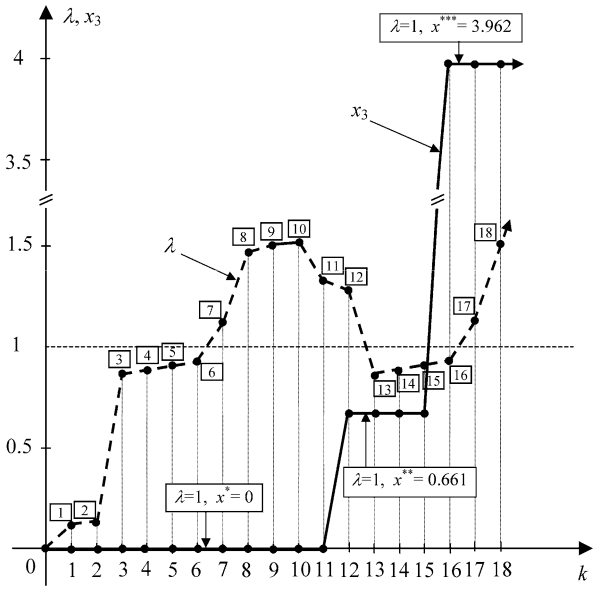


Fig. 11 Plots of λ and x_3 against the numbers of the computation steps k

3.2 Example 2

Let us consider the circuit shown in Fig. 12. The parameters of the Ebers–Moll model of the transistors are the same as in Example 1. The diode D_1 has the parameters: $I_S = 7.068$ fA, $V_T = 25.86$ mV, $R_D = 4\ \Omega$, where R_D is the contact resistor. To find the DC operating points, we apply the method developed in Sect. 2. For this purpose, the emitter and collector diodes are approximated by the circuit shown in Fig. 7b with the same parameters as in Example 1. The diode D_1 is also approximated by the circuit shown in Fig. 7b, with the parameters $R_1 = 33.511\ \Omega$, $R_2 = 5.187\ \Omega$,

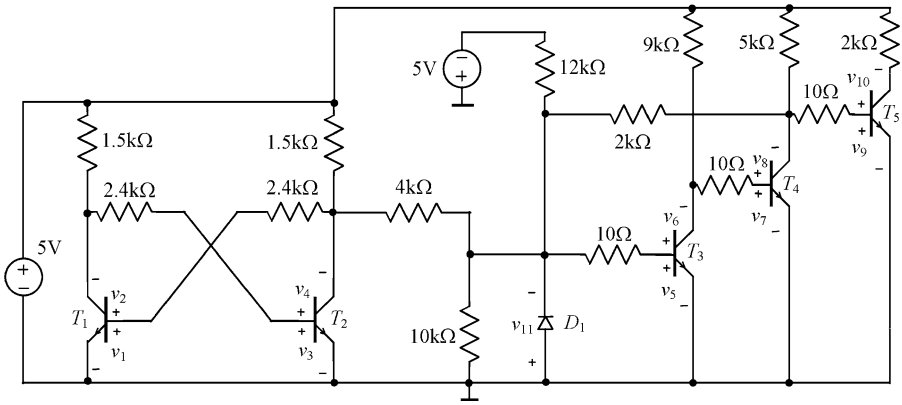


Fig. 12 Circuit for Example 2

$R_3 = 1$ GΩ, $V_0^{(1)} = 0.620$ V, $V_0^{(2)} = 0.783$ V, and the contact resistor $R_D = 4$ Ω connected in series.

The method developed in Sect. 2 gives five the following DC operating points:

$$\begin{aligned}
\tilde{\boldsymbol{v}}^{*} &= [0.106\ -3.258\ 0.747\ 0.641\ -0.387\ -1.085\ 0.693\ 0.636\ 0.056 \\
&\quad -4.943\ 0.387]^{\mathrm{T}}, \\
\tilde{\boldsymbol{v}}^{**} &= [0.719\ -0.057\ 0.715\ -0.071\ -0.202\ -0.904\ 0.696\ 0.635\ 0.061 \\
&\quad -4.939\ 0.202]^{\mathrm{T}}, \\
\tilde{\boldsymbol{v}}^{***} &= [0.744\ 0.629\ 0.114\ -2.682\ 0.341\ -0.368\ 0.705\ 0.632\ 0.072 \\
&\quad -4.927\ -0.341]^{\mathrm{T}}, \\
\tilde{\boldsymbol{v}}^{****} &= [0.744\ 0.630\ 0.114 -2.740\ 0.648\ -0.016\ 0.664\ -0.038\ 0.626 \\
&\quad -4.374\ -0.648]^{\mathrm{T}}, \\
\tilde{\boldsymbol{v}}^{*****} &= [0.744\ 0.630\ 0.114\ -2.742\ 0.655\ 0.617\ 0.038\ -0.701\ 0.731\ 0.635 \\
&\quad -0.655]^{\mathrm{T}},
\end{aligned} \tag{18}$$

where the elements of these vectors correspond to the voltages $v_1, v_2, \ldots, v_{11}$, in volts, indicated in Fig. 12. The CPU time is 0.022 s.

Using in succession each of the obtained solutions as the initial guess in the Newton–Raphson method we find the corrected operating points:

$$\begin{aligned}
\boldsymbol{v}^{*} &= [0.115\ -3.250\ 0.752\ 0.636\ -0.386\ -1.083\ 0.691\ 0.637\ 0.053 \\
&\quad -4.946\ 0.386]^{\mathrm{T}}, \\
\boldsymbol{v}^{**} &= [0.718\ -0.055\ 0.713\ -0.072\ -0.205\ -0.903\ 0.693\ 0.636\ 0.056 \\
&\quad -4.943\ 0.205]^{\mathrm{T}}, \\
\boldsymbol{v}^{***} &= [0.748\ 0.628\ 0.120\ -2.677\ 0.338\ -0.366\ 0.699\ 0.634\ 0.065
\end{aligned}$$

$$
\begin{aligned}
&-4.934\ -0.338]^{\mathrm{T}}, \qquad (19)\\
\boldsymbol{v}^{****} &= [0.749\ 0.629\ 0.119\ -2.736\ 0.649\ -0.020\ 0.669\ -0.042\ 0.627\\
&\quad -3.931\ -0.649]^{\mathrm{T}},\\
\boldsymbol{v}^{*****} &= [0.749\ 0.629\ 0.119\ -2.737\ 0.658\ 0.579\ 0.078\ -0.664\ 0.734\\
&\quad 0.635\ -0.659]^{\mathrm{T}}.
\end{aligned}
$$

Also, the SPICE simulator (ICAP/4) gives the same operating points, starting in succession from each at the solutions (18), rearranged into node voltages. They are close to the solutions obtained by the proposed method. The same results are obtained using the exhaustive method that guarantees finding all DC operating points [20].

3.3 Example 3

The circuit shown in Fig. 13 contains 51 transistors and 12 diodes. The parameters of the Ebers–Moll model of the transistors and the diodes are the same as in Example 2. The circuit is described by (5) where (3) consists of 114 individual equations.

To apply the method developed in Sect. 2, we approximate the emitter and collector diodes by the circuit shown in Fig. 6b with the following parameters:

Emitter diode: $R_1 = 4.539\ \Omega$, $R_2 = 1\ \mathrm{G}\Omega$, $V_0 = 0.678$ V,
Collector diode: $R_1 = 4.572\ \Omega$, $R_2 = 1\ \mathrm{G}\Omega$, $V_0 = 0.660$ V.

The diodes D_1–D_{12} are approximated by the same circuit with the parameters: $R_1 = 9.144\ \Omega$, $R_2 = 1\ \mathrm{G}\Omega$, $V_0 = 0.660$ V and the contact resistor $R_D = 4\ \Omega$ connected in series.

The method gives a unique DC operating point specified by a vector $\boldsymbol{v}$ consisting of the voltages $v_1, v_2, \ldots, v_{114}$. These results enable us to find node voltages in the circuit. Five of them, at the points A, B, C, D, E, are listed below:

$$\tilde{v}_A = -1.999\ \mathrm{V}, \quad \tilde{v}_B = 1.960\ \mathrm{V}, \quad \tilde{v}_C = 1.920\ \mathrm{V}, \quad \tilde{v}_D = -2.041\ \mathrm{V},$$
$$\tilde{v}_E = -2.643\ \mathrm{V}.$$

The CPU time is 0.162 s.

The Newton–Raphson or SPICE simulator used to correct the solutions lead to the following node voltages at the same points:

$$v_A = -1.996\ \mathrm{V}, \quad v_B = 1.927\ \mathrm{V}, \quad v_C = 1.855\ \mathrm{V}, \quad v_D = -2.070\ \mathrm{V},$$
$$v_E = -2.734\ \mathrm{V}.$$

Note The Newton–Raphson method applied to the circuit shown in Fig. 13, with the zero initial guess, does not converge in 1000 iterations.

4 Analysis of CMOS circuits

The method proposed in this paper can be extended to CMOS circuits as explained in the sequel.

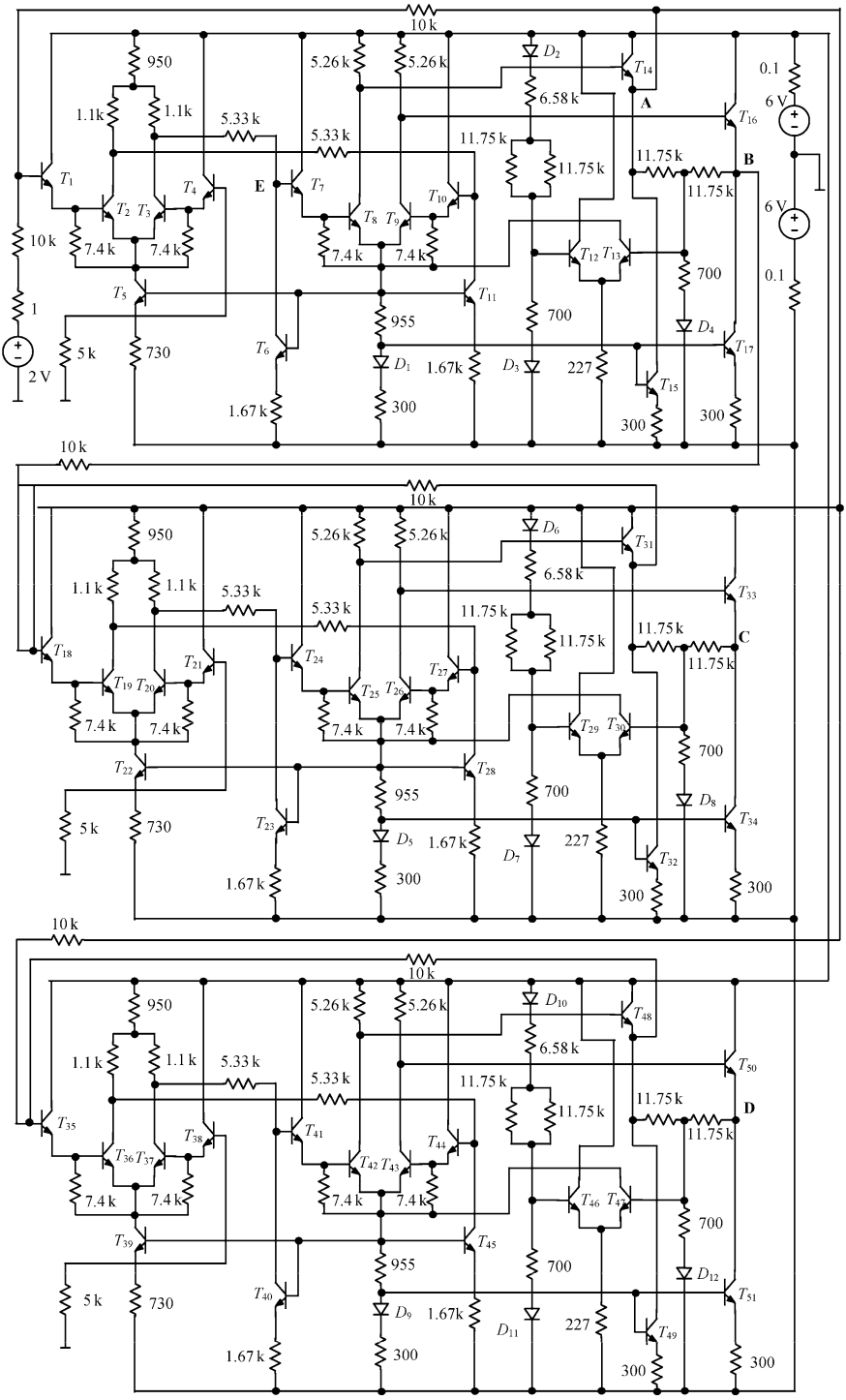


Fig. 13 The circuit for Example 3

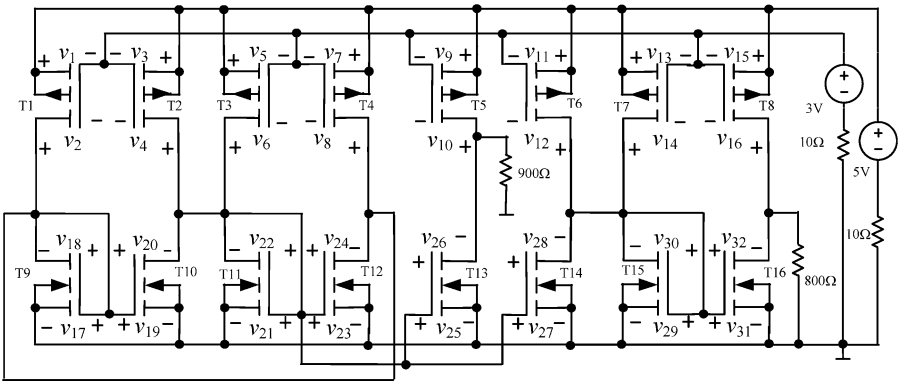


Fig. 14 CMOS circuit for Example 4

4.1 Example 4

Let us consider the circuit shown in Fig. 14. The MOS transistors are represented by the Shichman–Hodges model [14] built up in Level 1 of SPICE [12] with the following parameters: $R_D = R_S = 16.4\ \Omega$, $R_G = 0$, LAMBDA $= 0$, $v_{t_0} = 0.5705$ V for NMOS and -0.8351 V for PMOS, $K_p = 19.485\ \mu\text{A/V}^2$ for PMOS and $79.173\ \mu\text{A/V}^2$ for NMOS, $k = \frac{K_p}{2}\frac{W}{L} = 1\ \text{mA/V}^2$ for the transistors T4, T12 and $k = 0.5\ \text{mA/V}^2$ for the other transistors.

It can be shown [1, 17] that this model for n-channel MOS transistor is equivalent to the circuit depicted in Fig. 15, where the diodes are specified by equations

$$i_1 = \begin{cases} k(v_{gs} - v_{t_0})^2, & \text{for } v_{gs} \geq v_{t_0} \\ 0, & \text{for } v_{gs} < v_{t_0}, \end{cases} \tag{20}$$

$$i_2 = \begin{cases} k(v_{gd} - v_{t_0})^2, & \text{for } v_{gd} \geq v_{t_0} \\ 0, & \text{for } v_{gd} < v_{t_0}. \end{cases} \tag{21}$$

The current i_g in the model shown in Fig. 15 is forced to zero due to Kirchhoff's Current Law, which applied at node g gives

$$i_g = i_1 - 1 \cdot i_2 + i_2 - 1 \cdot i_1 = 0. \tag{22}$$

Consequently, value of the contact resistor R_G does not play any role in DC analysis and similarly as in IsSPICE we choose $R_G = 0$.

A similar model can be created for p-channel MOS transistors.

Since the diodes have the characteristics specified by (20) and (21) which coincide with the 0–v axis for $v < v_{t_0}$, their piecewise–linear model does not contain the branch consisting of a resistor only (R_2 in Fig. 6b or R_3 in Fig. 7b). Thus, the model consists of two parallel branches, each composed of the ideal diode, a resistor and a voltage source connected in series. If we add the third branch of the same type we obtain a model of the diode whose characteristic is approximated by a piecewise–linear 4-segment function. Such a model is used in this example with the following

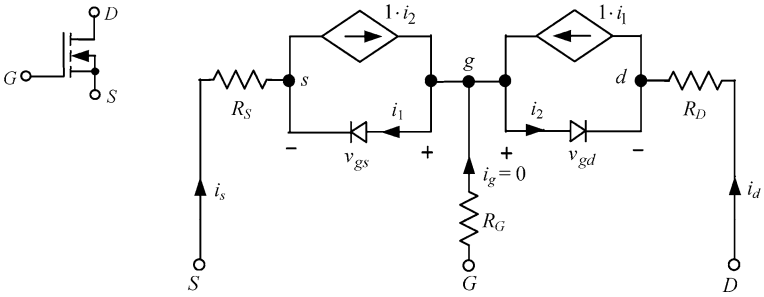


Fig. 15 Model of n-channel MOS transistor

parameters: $R_1 = 1305\ \Omega, V_0^{(1)} = 0.5705\ \text{V}, R_2 = 514.6\ \Omega, V_0^{(2)} = 1.45\ \text{V}, R_3 = 535.2\ \Omega, V_0^{(3)} = 2.4\ \text{V}$ for the NMOS transistor T12; $R_1 = 2062\ \Omega, V_0^{(1)} = 0.8351\ \text{V}, R_2 = 616.7\ \Omega, V_0^{(2)} = 1.45\ \text{V}, R_3 = 503.1\ \Omega, V_0^{(3)} = 2.4\ \text{V}$ for the PMOS transistor T4; $R_1 = 2611\ \Omega, V_0^{(1)} = 0.5705\ \text{V}, R_2 = 1029\ \Omega, V_0^{(2)} = 1.45\ \text{V}, R_3 = 1070\ \Omega, V_0^{(3)} = 2.4\ \text{V}$ for the NMOS transistors T9–T11, T13–T16; $R_1 = 4125\ \Omega, V_0^{(1)} = 0.8351\ \text{V}, R_2 = 1233\ \Omega, V_0^{(2)} = 1.45\ \text{V}, R_3 = 1006\ \Omega, V_0^{(3)} = 2.4\ \text{V}$ for the PMOS transistors T1–T3, T5–T8. Consequently, the method proposed in Sect. 2 can be applied to find DC operating points of the circuit. The method traces the homotopy path that intersects the $\lambda = 1$ plane at three points. As a result we obtain three DC operating points:

$$\begin{aligned}
\tilde{\boldsymbol{v}}^{*} = [&1.941\ -0.538\ 1.941\ -2.108\ 1.941\ -2.108\ 1.941\ -0.538\\
&1.941\ -2.517\ 1.941\ -0.901\ 1.941\ -0.901\ 1.941\ -2.741\\
&2.461\ 0.000\ 2.461\ 1.569\ 0.891\ 0.000\ 0.891\ -1.569\\
&0.891\ 0.408\ 0.891\ -1.207\ 2.099\ 0.000\ 2.099\ 1.840]^{\mathrm{T}},\\
\tilde{\boldsymbol{v}}^{**} = [&1.941\ -1.307\ 1.941\ -1.300\ 1.941\ -1.300\ 1.941\ -1.307\\
&1.941\ -2.715\ 1.941\ -1.307\ 1.941\ -1.307\ 1.941\ -2.735\\
&1.693\ 0.000\ 1.693\ -0.007\ 1.700\ 0.000\ 1.700\ 0.007\\
&1.700\ 1.415\ 1.700\ 0.007\ 1.693\ 0.000\ 1.693\ 1.428]^{\mathrm{T}},\\
\tilde{\boldsymbol{v}}^{***} = [&1.941\ -2.129\ 1.941\ -0.895\ 1.941\ -0.895\ 1.941\ -2.129\\
&1.941\ -2.726\ 1.941\ -1.787\ 1.941\ -1.787\ 1.941\ -2.595\\
&0.871\ 0.000\ 0.871\ -1.233\ 2.104\ 0.000\ 2.104\ 1.233\\
&2.104\ 1.831\ 2.104\ 0.891\ 1.213\ 0.000\ 1.213\ 0.808]^{\mathrm{T}},
\end{aligned} \tag{23}$$

where the components of the above vectors are the voltages $v_1, \ldots, v_{32}$ in volts, indicated in Fig. 14. The CPU time is 0.16 s. Correcting each of the operating points by the Newton–Raphson algorithm or SPICE simulator yields the results close to (23):

$$\boldsymbol{v}^{*} = [1.945\ -0.544\ 1.945\ -2.159\ 1.945\ -2.159\ 1.945\ -0.544$$

$$
\begin{aligned}
&1.945\ -2.487\ 1.945\ -0.877\ 1.945\ -0.877\ 1.945\ -2.768\\
&2.455\ 0.000\ 2.455\ 1.614\ 0.840\ 0.000\ 0.840\ -1.614\\
&0.840\ 0.328\ 0.840\ -1.281\ 2.122\ 0.000\ 2.122\ 1.891]^{\mathrm{T}},\\
\boldsymbol{v}^{**} = [&1.945\ -1.318\ 1.945\ -1.318\ 1.945\ -1.318\ 1.945\ -1.318\\
&1.945\ -2.703\ 1.945\ -1.318\ 1.945\ -1.318\ 1.945\ -2.723\\
&1.681\ 0.000\ 1.681\ 0.000\ 1.681\ 0.000\ 1.681\ 0.000\\
&1.681\ 1.384\ 1.681\ 0.000\ 1.681\ 0.000\ 1.681\ 1.404]^{\mathrm{T}},\\
\boldsymbol{v}^{***} = [&1.945\ -2.167\ 1.945\ -0.875\ 1.945\ -0.875\ 1.945\ -2.167\\
&1.945\ -2.755\ 1.945\ -1.896\ 1.945\ -1.896\ 1.945\ -2.618\\
&0.832\ 0.000\ 0.832\ -1.292\ 2.124\ 0.000\ 2.124\ 1.292\\
&2.124\ 1.879\ 2.124\ 1.020\ 1.103\ 0.000\ 1.103\ 0.722]^{\mathrm{T}}.
\end{aligned}
\tag{24}
$$

4.2 Example 5

Let us consider the circuit shown in Fig. 16. The MOS transistors are represented as in Example 4 with the following parameters: $k = 1$ mA/V^2 for the transistors T2, T5–T10, $k = 3.333$ mA/V^2 for the transistor T1, $k = 0.416$ mA/V^2 for the transistor T3, $k = 8$ mA/V^2 for the transistor T4.

The diodes included in the model of MOS transistors (see Fig. 15) are represented by similar circuit as in Example 4 with the following parameters:

NMOS transistors T2, T6, T8, T10: $R_1 = 1049\ \Omega$, $V_0^{(1)} = 0.5705$ V, $R_2 = 407.7\ \Omega$, $V_0^{(2)} = 1.7$ V, $R_3 = 291.6\ \Omega$, $V_0^{(3)} = 3$ V.

PMOS transistors T5, T7, T9: $R_1 = 1462\ \Omega$, $V_0^{(1)} = 0.8351$ V, $R_2 = 433.5\ \Omega$, $V_0^{(2)} = 1.74$ V, $R_3 = 313.5\ \Omega$, $V_0^{(3)} = 3$ V.

PMOS transistor T1: $R_1 = 438.6\ \Omega$, $V_0^{(1)} = 0.8351$ V, $R_2 = 125.7\ \Omega$, $V_0^{(2)} = 1.74$ V, $R_3 = 102.6\ \Omega$, $V_0^{(3)} = 3$ V.

PMOS transistor T3: $R_1 = 3509\ \Omega$, $V_0^{(1)} = 0.8351$ V, $R_2 = 1005\ \Omega$, $V_0^{(2)} = 1.74$ V, $R_3 = 821.2\ \Omega$, $V_0^{(3)} = 3$ V.

NMOS transistor T4: $R_1 = 131.2\ \Omega$, $V_0^{(1)} = 0.5705$ V, $R_2 = 50.96\ \Omega$, $V_0^{(2)} = 1.7$ V, $R_3 = 36.45\ \Omega$, $V_0^{(3)} = 3$ V.

The method traces the homotopy path that intersects the $\lambda = 1$ plane at three points. As a result, we obtain three DC operating points:

$$
\begin{aligned}
\tilde{\boldsymbol{v}}^{*} = [&2.495\ 2.025\ 2.500\ -2.025\ 2.495\ -2.417\ 2.500\ 2.417\\
&0.469\ 0.469\ 0.083\ -4.912\ 4.995\ 4.995\ 0.000\ -4.995\\
&0.000\ -4.995\ 4.995\ 4.995]^{\mathrm{T}},\\
\tilde{\boldsymbol{v}}^{**} = [&2.489\ 2.019\ 2.500\ -2.019\ 2.489\ -2.417\ 2.500\ 2.417\\
&0.469\ -2.163\ 0.082\ -2.273\ 2.633\ 0.000\ 2.356\ 0.000
\end{aligned}
$$

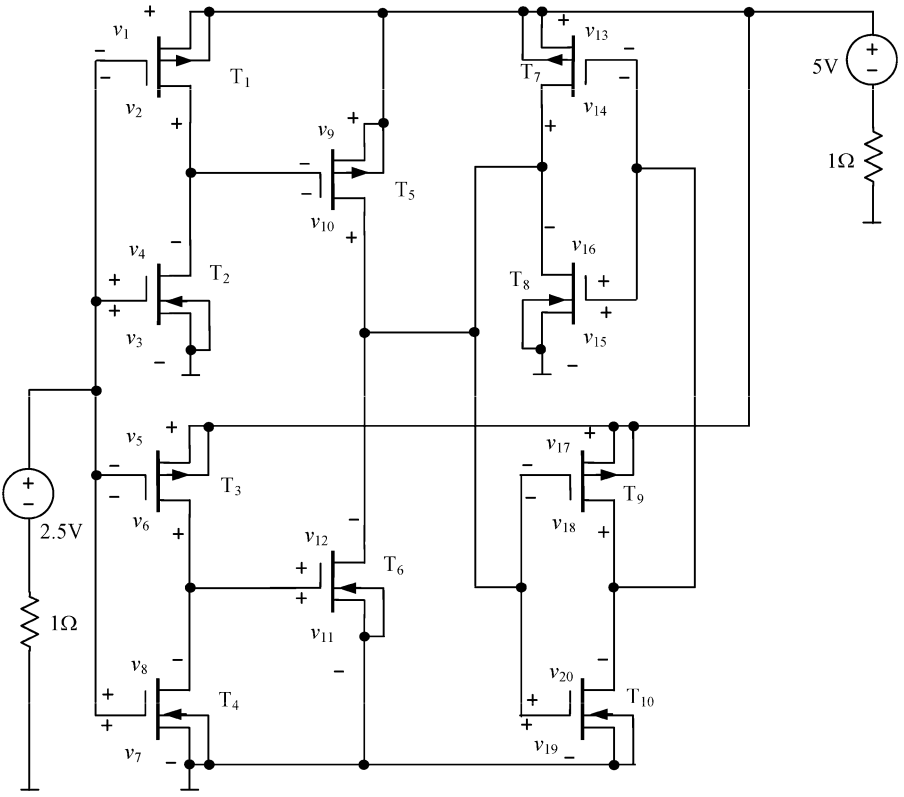


Fig. 16 CMOS circuit for Example 5

$$\begin{aligned}
&2.633\ 0.000\ 2.356\ 0.000]^{\mathrm{T}}, \qquad (25)\\
\tilde{\boldsymbol{v}}^{***} = [&2.495\ 2.025\ 2.500\ -2.025\ 2.495\ -2.417\ 2.500\ 2.417\\
&0.469\ -4.525\ 0.083\ 0.083\ 0.000\ -4.995\ 4.995\ 4.995\\
&4.995\ 4.995\ 0.000\ -4.995]^{\mathrm{T}},
\end{aligned}$$

where the components of the above vectors are the voltages $v_1, \ldots, v_{20}$ indicated in Fig. 16. The CPU time is 0.065 s. Correcting each of the operating points by the Newton–Raphson algorithm or SPICE simulator yields the results close to (25):

$$\begin{aligned}
\boldsymbol{v}^{*} = [&2.495\ 1.950\ 2.500\ -1.950\ 2.495\ -2.426\ 2.499\ 2.426\\
&0.544\ 0.544\ 0.073\ -4.921\ 4.995\ 4.995\ 0.000\ -4.995\\
&0.000\ -4.995\ 4.995\ 4.995]^{\mathrm{T}},\\
\boldsymbol{v}^{**} = [&2.489\ 1.941\ 2.500\ -1.941\ 2.489\ -2.426\ 2.499\ 2.426\\
&0.547\ -2.079\ 0.073\ -2.288\ 2.626\ 0.000\ 2.362\ 0.000 \qquad (26)\\
&2.626\ 0.000\ 2.362\ 0.000\ ]^{\mathrm{T}},
\end{aligned}$$

$$\boldsymbol{v}^{***} = [2.495\ 1.950\ 2.499\ -1.950\ 2.495\ -2.426\ 2.499\ 2.426\ 0.544\ -4.450\ 0.073\ 0.073\ 0.000\ -4.995\ 4.995\ 4.995\ 4.995\ 4.995\ 0.000\ -4.995]^{\mathrm{T}}.$$

5 Conclusion

The method proposed in this paper is universal and enables us to analyze piecewise–linear BJT and CMOS circuits having a unique or multiple DC operating points. Since the method operates in succession on individual equations rather than sets of equations, it is very fast and does not require large computation power. Numerical examples show that it is remarkably efficient. For different vectors $\boldsymbol{d}$, obtained using the procedure described in Sect. 2, different homotopy paths are traced. Occasionally it may occur that the homotopy path crosses the $\lambda = 1$ plane at less number of points than the number of the solutions. Therefore, if the number of the DC operating points is not known in advance, we should apply the method at a few different vectors $\boldsymbol{d}$ and collect all the obtained solutions. However, in the performed numerical experiments usually all the DC operating points of the circuits were obtained using the vector $\boldsymbol{d}$ selected for the first time.

Acknowledgements This work was supported by the National Science Centre under Grant UMO-2011/01/B/ST7/06043.

The authors would like to thank Dr. Stanislaw Halgas for help with choice and verification of the numerical examples, and the anonymous reviewers for useful and constructive comments which have improved this paper.

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