HPPC 2010: Forth Workshop on Highly Parallel Processing on a Chip

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Foreword

In response to the stagnant growth in conventional, single-processor performance increased on-chip parallelism is seen as a solution to the demands for high performance and power efficiency for general purpose, mainstream computing. While many general-purpose architectures with a moderate number of processing cores are already on the market, architectures with much more significant on-chip parallelism are generally expected, as is already seen for many special purpose processors. How the processing power of such many-core systems can be leveraged for general purpose computing is a most critical and completely open issue, as witnessed by the lack of convergence towards standard architecture and programming models. A major challenge for the coming years therefore is the design of highly parallel single-chip architectures that can support manageable programming abstractions to allow the mainstream programmer to take advantage of the processing power furthered by the technological developments.

The workshop on *Highly Parallel Processing on a Chip* (HPPC), now in its 4th incarnation, is dedicated to the interface between single-chip/node multi/many-core architectures and programming paradigms, models, and languages towards supporting parallel algorithms and applications development in an efficient and manageable way. HPPC is a forum for **bold**, *new* ideas on architectural organization (general- and special-purpose processors, heterogeneous designs, memory organization, on-chip communication networks, etc.), parallel programming models, languages, and libraries, many-core parallel algorithms, and application studies on both existing and envisaged architectures.

In response to the call-for-papers that was issued early in 2010, HPPC 2010 received 18 submissions that were all of relevance to the general workshop themes. Based on relevance and quality of the submissions as judged by the program committee (which did most of the reviewing with few external reviewers) this year a slightly higher number of papers than in previous years were selected for presentation by the program chairs. This made for an acceptance rate of 44%, which is not a measure of anything, anyway, in case this bothers anyone.

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The workshop organizers and program chairs thank sincerely all contributing authors, and hope that they will also find it worthwhile to submit contributions next year. Most contributions received *four* reviews (which is what HPPC strives for), a few having only three (which we regret), and were thus given an all in all fair consideration. The members of the program committee are likewise all thanked for the time and expertise they put into the reviewing work, and for getting it done within the rather strict time limit.

The Euro-Par 2010 workshop day featured a number of workshops, and was very lively, well-attended and generally well-organized. The HPPC workshop was conducted in an informal atmosphere and gave, hopefully, enough room for interaction and discussion between presenters and audience. HPPC 2010 had a high, cumulative attendance of more than 70. In addition to the 8 contributed talks, the workshop featured two longer, invited talks by Rolf Hoffmann (on "The massively parallel computing model CGA") and Jim Held (on "Single-chip Cloud Computer, an IA tera-scale research processor"). The workshop organizers thank all attendees, who contributed much to the workshop with questions, comments and discussion, and hope they found something of interest in the workshop, too. We also thank the Euro-Par organization for creating the opportunity to arrange the HPPC workshop in conjunction with the Euro-Par conference, and of course all Euro-Par 2010 organizers for their help and support both before and during the workshop. HPPC sponsors VTT, University of Vienna, and Euro-Par 2010 are warmly thanked for the financial support that made it possible to invite Rolf Hoffmann and Jim Held, both of whom we sincerely thank for accepting our invitation to speak and for their excellent talks.

These post-workshop proceedings include the final versions of the presented HPPC 2010 papers (accepted papers not presented at the workshop will not be included in the proceedings, but HPPC 2010 had all authors present and presenting), taking the feedback from reviewers and workshop audience into account. In addition to the reviews by the program committee prior to selection, an extra, post-workshop (blind) "*reading*" of each presented paper by one of the other presenters has been introduced with the aim of getting fresh, uninhibited high-level feedback for the authors to use at their discretion in preparing their final version (no papers would have been rejected at this stage – bar major flaws). This idea was introduced with HPPC 2008, and will be continued also for HPPC 2011.

The contributed papers are printed in the order they were presented at the workshop. A full version of the invited talk by Rolf Hoffmann and an abstract of Jim Held's talk have also been included in the proceedings. Thematically, the contributed papers cover aspects of memory organization ("Evaluation of low-overhead organizations for the directory in future many-core CMPs" by Ros and Acacio), programmability ("A work stealing scheduler for parallel loops on shared cache multicores" by Tchiboukdjian, Danjean, Gautier, Le Mentec and Raffin, "Resource-agnostic programming for many-core microgrids" by Bernard, Grelck, Hicks, Jesshope and Poss, "Programming heterogeneous multicore systems using Threading Building Blocks" by Russell, Keir, Donaldson, Dolinsky, Richards

and Riley), applications and optimization for accellerators and special processors ("Fine-grain parallelization of a Vlasov-Poissoin application on GPU" by Latu, "Highly parallel implementation of Harris corner detector on CSX SIMD architecture" by Hosseini, Fijany and Fontaine, "Static speculation as post-link optimization for the Grid Alu Processor" by Jahr, Shehan, Uhrig and Ungerer), and on-chip networks and routers ("A multi-level routing scheme and router architecture to support hierarchical routing in large network on chip platforms" by Holsmark, Kumar and Palesi).

The HPPC workshop is planned to be organized again in conjunction with Euro-Par 2011.

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