

Key Microarchitectural Innovations for Future Microprocessors

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Abstract. Microprocessors have experienced tremendous performance improvements generation after generation since its inception. Moores law has fueled this evolution and will keep doing it in forthcoming generations. However, future microprocessors are facing new challenges that require innovative approaches to keep delivering improvements comparable to those that we have enjoyed so far. Power dissipation is a main challenge in all segments, from ultra-mobile to high-end servers. Another important challenge is the fact that we have relied on instruction-level parallelism (ILP) as a main lever to improve performance, but after more than 30 years of enhancing ILP techniques we are approaching a point of diminishing returns. In this talk we will discuss these challenges and propose some solutions to tackle them. Multicore is a recently adopted approach in most microprocessors that offers significant advantages in terms of power and exploits a new source of parallelism: thread-level parallelism. In this talk we will discuss the benefits of multicore and also show its limitations. We will also describe some other technologies that we believe are needed to complement the benefits of multicore and offer all together a foundation for future microprocessors.