Simulation-Based 'Smart' Operation Management System for Semiconductor Manufacturing

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Abstract. Presented in this paper is a framework of a simulation-based 'smart' operation management system (OMS) for semiconductor manufacturing. Also described are changes in the semiconductor market environment and key modules in the smart OMS. The proposed smart OMS is being implemented for a couple of IC chip makers in Korea.

Keywords: Simulation-based operation management system · Online simulation · Lot pegging · Fab scheduling

1 Introduction

Online simulation is used in the simulation-based operational management. An *online simulation* starts with the current state of manufacturing facilities at any point in time. A simulation-based operation management system (OMS) provides stakeholders with the ability to evaluate the capacity of the facility for new orders and to predict the expected delivery times and changes in operations [1–3].

In recent years, the semiconductor industry has been forced to become more competitive in pricing and in adopting new technology, while delivering IC chips faster and with an enhanced CPFR (collaborative planning forecasting and replenishment) with their customers. Thus, in order to meet the requirements of competitive pricing, fast-delivery, and CPFR, the OMS for semiconductor manufacturing should be capable of (1) increasing the number of tools per worker for TAT (turn-around-time) reduction, (2) enhancing the visibility of the supply chain, (3) providing reliable RTF (return to forecast) values, (4) minimizing WIP, (5) maximizing resource utilization, and (6) increasing the global efficiency of the IC chip supply chain.

Presented in the paper is an overall framework, together with some technical details, of a simulation-based 'smart' OMS for semiconductor manufacturing. Changes in the semiconductor market environment and in the concept of 'smart' OMS are given in the next section, and the architecture of the smart OMS is detailed in Sect. 3. Descriptions of the key modules in the smart OMS are given in Sect. 4, followed by a final section on conclusions and discussion.

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2 Semiconductor Market Environment and 'Smart' Operation Management System

Depicted in Fig. 1 are changes in the IC chip market environment. In the case of memory chips, there are only a few major suppliers (like Samsung and Micron) and a few major customers. The customers of IC chips (like Apple and HP) are now producing their products via *mass customization,* which requires low unit costs of mass production as well as swiftness in model changes and new product introduction, which in turn require the IC chip makers to become more competitive in pricing and in adopting new technology, while delivering IC chips faster with an enhanced CPFR with their customers.

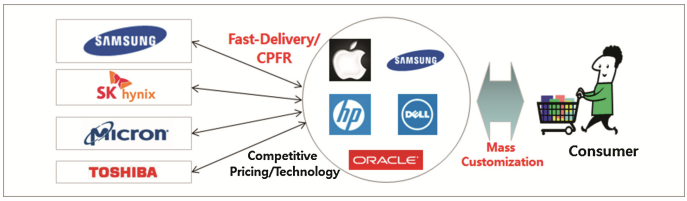

Fig. 1. Changes in the semiconductor market environment

In order to enhance an IC chip maker's competitive power for ***pricing***, its Fab *operation management system* (OMS) should be able to

(1) minimize WIP to reduce TAT and to avoid deterioration defects,
(2) increase the *number of tools per worker* (NTPW) to reduce TAT and labor costs,
(3) maximize resource utilization, and
(4) increase global efficiency of the IC chip supply chain.

For the ***fast delivery*** of IC chips, the OMS should be able to

(1) minimize TAT by minimizing WIP and maximizing NTPW, and
(2) enhance the visibility (or transparency) of the IC chip supply chain.

For efficient ***CPFR*** with customers, the OMS should be able to

(1) enhance the visibility of the supply chain,
(2) provide reliable return-to-forecast (RTF) values, and
(3) minimize TAT.

In summary, in order to meet the three requirements (competitive pricing, fast-delivery, and CPFR), an OMS for semiconductor manufacturing should be capable of (1) increasing the number of tools per worker for TAT reduction, (2) enhancing the visibility of the supply chain, (3) providing reliable RTF values, (4) minimizing WIP, (5) maximizing resource utilization, and (6) increasing the global efficiency of the IC chip supply chain. Such an OMS is often referred to as a 'smart' OMS. It is well observed in semiconductor industry that TAT decreases drastically as the number of tools per worker increases.

Figure 2 illustrates the concept of such a smart OMS. A smart OMS is similar to a smart phone GPS navigation which receives the current car location from the GPS and the current traffic information from the ITS (intelligent transportation system) and provides real-time information and advice to the driver. The smart OMS of a semiconductor Fab (or of the entire supply chain) generates production target values and provides relevant data and advice to stakeholders in 'real-time' by making *online simulation* runs in real-time with minimal human intervention.

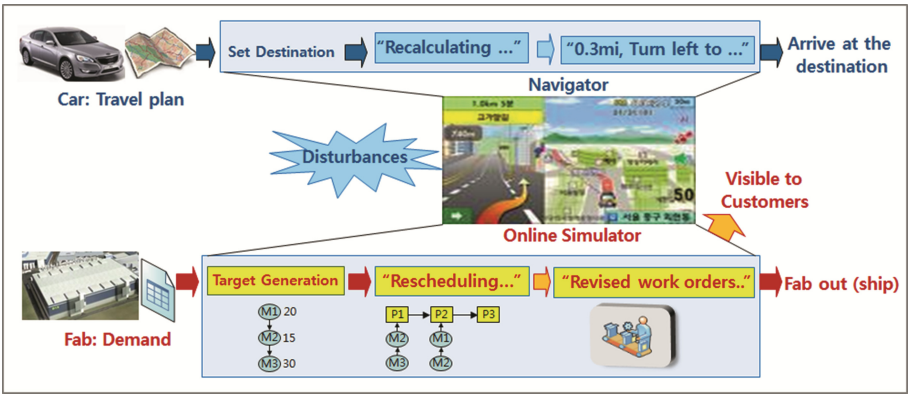

Fig. 2. Concept of a smart operation management system (OMS)

3 Architecture of Smart Operation Management System for Semiconductor Manufacturing

The smart OMS depicted in Fig. 2 is a simulation-based OMS. Perhaps, the concept of a simulation-based OMS was first proposed by the first author of this paper in an IFIP WG 5.7 conference [1]. OMSs were (and still are) often referred to as *manufacturing execution systems* (MES). More recently, a simulation-based OMS for LCD module manufacturing was presented [2]. Figure 3 shows the flow of LCD module manufacturing and the overall architecture of its simulation-based OMS.

When a weekly MP (master plan) is issued by the SCP (supply chain planner) system, the Weekly Planning System performs finite capacity planning to generate feasible daily production plans for the DPS (daily planning and scheduling) system. The DPS system generates detailed loading schedules for the TFT (thin-film-transistor) Fab, CF (color filter) Fab, LC (liquid crystal) Fab, and Module line. The weekly planning system (WPS) receives the weekly MP from the SCP system once a week and performs finite capacity planning to generate feasible daily production plans, purchase orders for the suppliers, etc.

Figure 4 shows the structure of a typical IC chip supply chain (or manufacturing network). A semiconductor wafer goes through a series of fabrication steps in a Fab to form a large number of ICs on its face (for 30–40 days) and stays in a Probe line to be

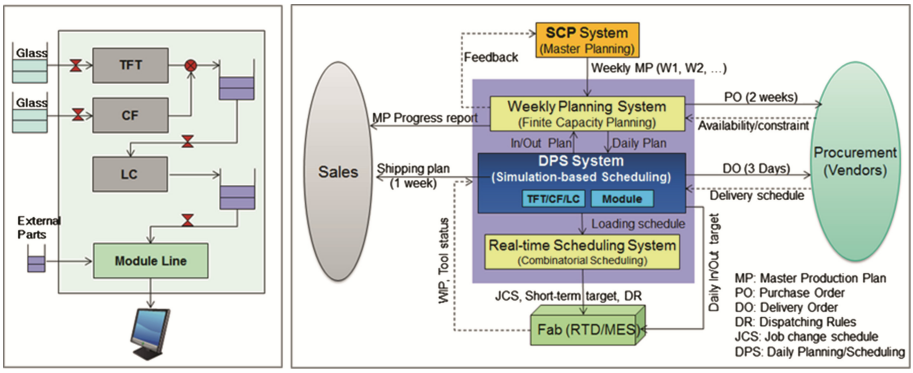

Fig. 3. Architecture of the simulation-based OMS for LCD module manufacturing [2]

probed for possible defects (for 2–5 days). Then, the chips are put into an IC package in the back end lines (for 3–7 days). A group of Fabs that can share resources is called a *site*. IC chips fabricated and probed in domestic Fabs may be sent to an overseas back-end line for packaging, and vice versa.

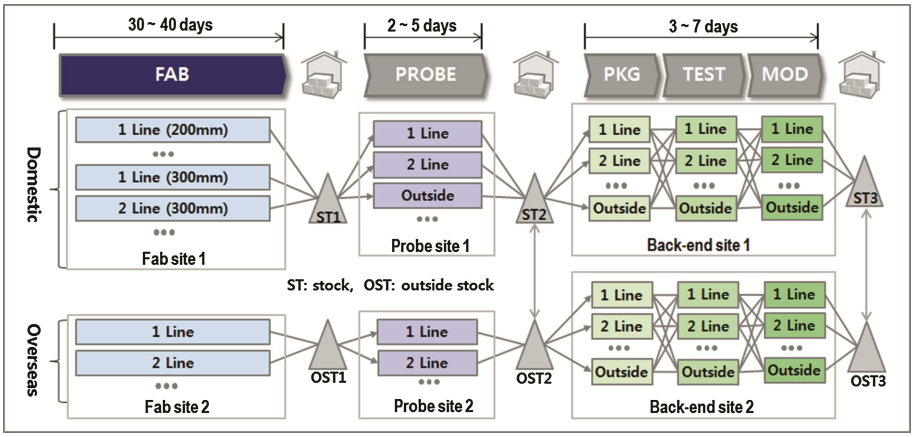

Fig. 4. Structure of IC chip supply chain

Shown in Fig. 5 is the overall architecture of the simulation-based OMS for IC chip manufacturing; this architecture corresponds to the supply chain structure shown in Fig. 4. The OMS consists of four software modules: the *Factory Planner* for generating daily input and output plans, the *Lot Pegging Module* for pegging the lots and generating their step targets and RTF values, the *What-if Simulator* for estimating bottleneck steps and WIP, and the *Fab Scheduler* for generating tool schedules. The Master Planning System (MPS) generates *weekly targets* for the Factory Planner and *demand data* for the Lot Pegging Module based on the firm *orders* and *forecast* values from Marketing and Sales. The key outputs from the OMS are (1) tool schedules to Real-Time

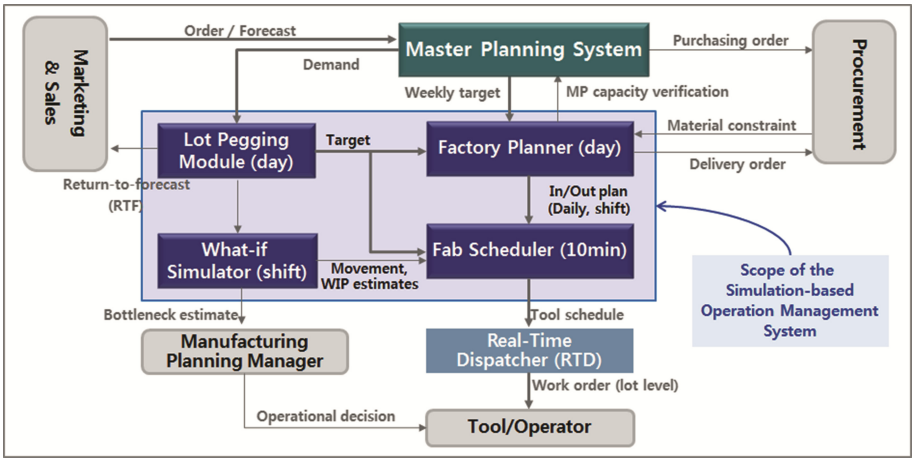

Fig. 5. Architecture of simulation-based OMS for IC chip manufacturing

Dispatchers (RTD), (2) RTF to Marketing and Sales, (3) delivery orders to Procurement, and (4) Master Plan verification back to MPS.

The *Factory Planner* is executed once a day for a simulation time period of 2–7 days at each site (e.g., Fab site 1, Probe site 1, etc., as shown in Fig. 4); the *Lot Pegging Module* is executed daily for all the lots in the supply chain, as shown in Fig. 4. The *What-if Simulator* is executed at the beginning of each shift for a simulation time period of 1–2 shifts at each line (it may be executed every hour if necessary). The *Fab Scheduler* is executed every ten minutes for a simulation time period of one shift for each line. The RTDs generate lot-level work orders (to each of the individual tools and operators) in real-time (less than 2 s).

The simulation-based OMS presented in Fig. 5 is a 'smart' OMS in the sense that (1) it is executed with minimal human intervention, (2) the current status and future trajectories of the supply chain are always visible to all stakeholders and (3) 'optimal' work orders are generated in real time. 'Optimal' work orders should maximize *step movements* and minimize both *WIP* and *TAT,* while also minimizing their variability.

4 Modules in the Smart OMS for Semiconductor Manufacturing

Some details of the individual modules of the OMS depicted in Fig. 5 are described in this section. Topics to be covered here are lot pegging, factory planning simulation, what-if simulation, and Fab scheduling simulation.

As shown in Fig. 6, *lot pegging* is carried out backward starting from the IC chip *Demand* data, through Probe stages, to the final *Fab-in target* stage, in which the blank wafers are released into the Fab. The lot pegging system keeps track of the progress of any given lot: (1) it provides the latest process start time (LPST) for each pegged lot to meet its demand; (2) it detects unpegged lots that have no demand; and (3) it provides

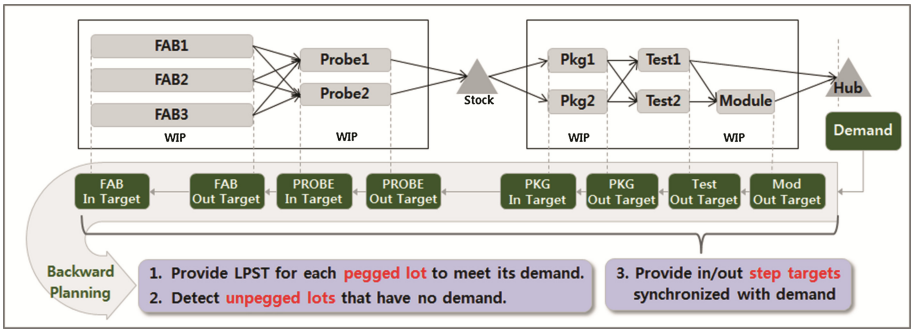

Fig. 6. Lot pegging operation

in/out step targets synchronized with demand. Through this system, any excess WIP without a target can be identified and controlled.

How factory planning simulation is carried out by the *Factory Planner* is shown in Fig. 7. The system generates an optimized plan for each line that ultimately satisfies the customers' demands. To generate the in and out plans for each line, factory planning simulation is carried out in two steps starting from the demand data: Target Generation via backward planning simulation [4] and Capacity Planning via a forward planning simulation [5]. The final outputs from the factory planning simulation are the estimated step completion times, machine (i.e., tool) schedules, and Fab out plans for each and every line in the supply chain.

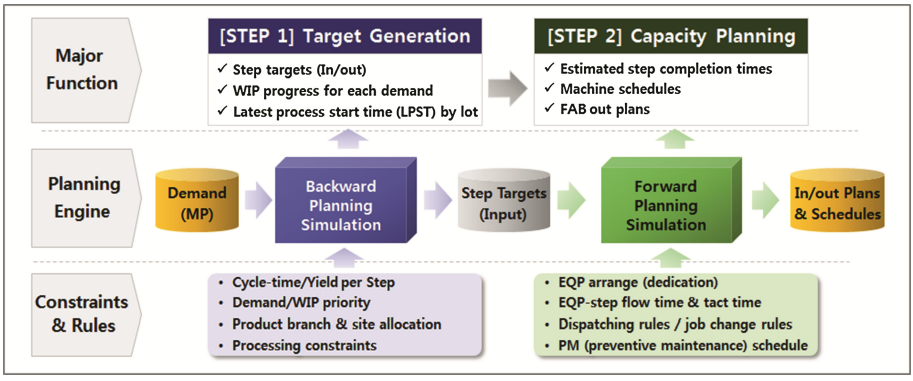

Fig. 7. Business architecture of the factory planner

Figure 8 shows the business architecture of the *What-if Simulator*. The simulation engine receives three types of input: Master data (product/BOP model, equipment model, and job change model); current status data (WIP, equipment, and PM); and production plan data (step targets and release plans). Then, it generates four types of KPI data: step movement estimates, Fab-out estimates, WIP level estimates, and expected bottleneck steps. As shown in the right part of Fig. 8, the system provides various decision-support data to the line managers. It also provides various technical

data to the execution modules of the OMS, such as the RTD/MES (manufacturing execution system), Fab scheduler, and PM (preventive maintenance) scheduler. How the what-if simulation is performed by the simulation engine may be found in [6, 7].

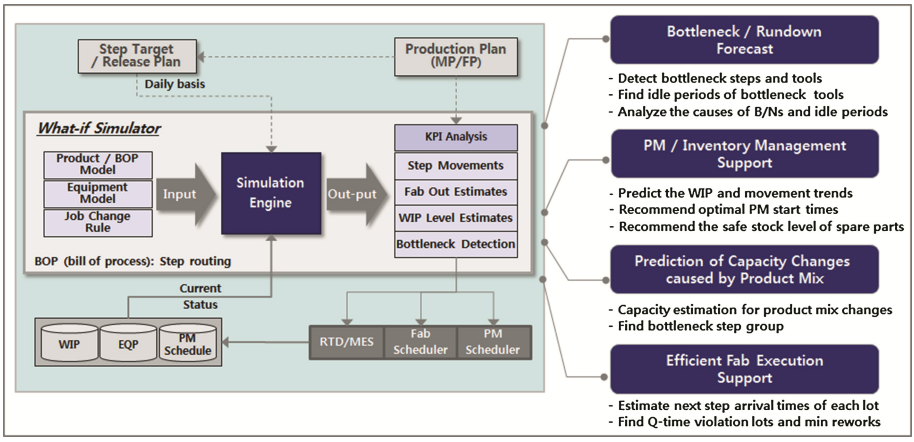

Fig. 8. Business architecture of the What-if simulator

The *Fab Scheduler* generates release plans and tool schedules such that the step targets provided by the Lot Pegging Module and Factory Planner are satisfied. First, the release plan for the line is generated considering capacity constraints, equipment arrangement (i.e., dedication), and operational rules. Then, a loading simulation, which is the same as the forward planning simulation shown in Fig. 7, is carried out to generate tool schedules. Figure 9 shows the major IC-chip processing steps for which tool schedules are generated.

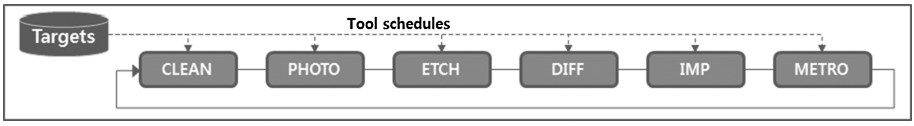

Fig. 9. Major processing steps for IC chip manufacturing

5 Summary and Conclusion

Presented in the paper is a framework of a simulation-based 'smart' operation management system (OMS) for semiconductor manufacturing. Also described are changes in the semiconductor market environment and key modules in the smart OMS. The proposed smart OMS is being implemented for a couple of IC chip makers in Korea. IC Chip manufacturing is generally classified into memory semiconductors and non-memory semiconductors. The latter are produced in much more varieties and smaller quantities than the former. Moreover, the overall production consists of numerous

production process flows. Non-memory semiconductors especially have a higher rate of sample runs and/or engineering lots in the Fab, and require delivery management on a per lot basis.

The smart OMS architecture presented in this paper is applicable for non-memory semiconductors (often referred to as system LSI) as well. In detail, for non-memory semiconductors, it is critical to manage the delivery of each demand using the lot pegging module and the FAB Scheduler has to use a loading simulation logic that can reflect the variety of process flows of each product on a per lot basis. The proposed smart OMS is being implemented for a couple of IC chip makers in Korea and the prospects so far are quite promising; however, more rigorous analysis and evaluation of the proposed OMS have yet to be made.

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