

Formal Verification - Applications & Case Studies

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Chrysalis is delivering formal verification products and support to over sixty customer sites world-wide. Design VERIFYer(r) software is an equivalence checking tool that proves the functional equivalence of two design descriptions. It is being applied to a variety of steps in the design process. This paper will include example applications that include RTL to gate, gate to gate, gate to switch, and RTL to switch comparisons. A case study that demonstrates the success of Design VERIFYer for a customer's verification requirements throughout the design process will be presented. Included in the case study are examples of applications stated above. This paper will also describe our recently introduced Design INSIGHT(r) formal RTL design tools for model checking and symbolic simulation which enable customers to complete correct RTL designs faster than with simulation alone.