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40-Gb/s all-optical digital 4-bit priority encoder employing cross-gain modulation in semiconductor optical amplifiers

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High-speed all-optical logic circuits have attracted much attention because of their important roles in signal processing in next-generation optical networks. The digital encoder is widely used in binary calculation, multiplexing, demultiplexing, address recognition and data encryption. A priority encoder allows the existence of multiple valid inputs simultaneously, identifies the priority of the request signals and encodes the priority. We propose and experimentally demonstrate an all-optical 4-bit priority encoder for return-to-zero signals at 40 Gbit/s based on cross-gain modulation in semiconductor optical amplifiers. Detuning filters after semiconductor optical amplifiers are employed to improve the output performance. Correct logic bit sequences and clear open eye patterns with extinction ratios exceeding 10 dB are achieved.

all-optical logic gates, delay interferometers, semiconductor optical amplifier

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High-speed all-optical logic circuits will be widely used in next-generation optical networks because of their important roles in signal processing such as address recognition, data encryption and label swapping. Recently, various basic logic gates have been demonstrated with different nonlinear devices [1–3]. Meanwhile, many more complex all-optical logic circuits have also been reported. For combinational logic functions, a 10-Gb/s all-optical half-adder with interferometric semiconductor optical amplifier (SOA) gates has been demonstrated [4], a simultaneous optical digital half-subtractor and adder using SOAs combined with a waveguide made from periodically poled lithium niobate has been proposed [5], an all-optical encoder and comparator were realized simultaneously for two-input return-to-zero (RZ) signals at 40 Gbit/s on the basis of cross-gain modulation (XGM) and four-wave mixing (FWM) in three parallel SOAs [6], and a 2-to-4 level decoder was used to develop an all-optical two-input digital multiplexer based on cross polarization modulation in an SOA [7]. Sequential logic circuits, such as an N-bit shift register [8] and binary counter [9], were designed and demonstrated exploiting ring buffers. On the other hand, logic minterms were reported [10,11] for three-input demodulated differential phase-shift keying signals employing SOAs and delay interferometers (DIs) at 20 and 40 Gbit/s respectively, which can be considered a basic building block for arbitrary logic functions. However, to our best knowledge, a module that performs digital priority encoding in the optical domain has not yet been demonstrated.

It is known that a traditional digital binary encoder enables only one effective input at any one time. If more than one input is present at the same time, the circuit will miscode. However, in a practical situation, different inputs require responses simultaneously; e.g., the interrupt request in computer systems. A priority encoder allows the existence of multiple valid inputs simultaneously, identifies the priority of the request signals and encodes the priority.

In this paper, we demonstrate an all-optical 4-bit priority encoder operating at 40 Gbit/s based on XGM in SOAs. Detuning filters were employed after SOAs to improve dy-

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namic characteristics. The proposed scheme has the advantages of power efficiency, high operation speed and integration potential.

1 Principle of operation

The logic truth table for an all-optical digital 4-bit priority encoder is shown in Table 1. I_3, I_2, I_1 and I_0 are four line inputs, and the logic state "1" indicates that a response is required while the logic state "0" indicates that it is not. "×" is an arbitrary item that could be "1" or "0". Y_1 and Y_0 are the final outputs encoded according to the priority of the signals requiring a response. With regard to a stable system, the output is "0" if there is no input. Therefore, Y_1Y_0 is "00" if $I_3I_2I_1I_0 = 0000$. However, this conflicts with the output encoding when $I_3I_2I_1I_0 = 0001$. Thus, GS is set to identify whether there are inputs, and it gives the system a warning output, logic state "1", if the input is 0000. In this circumstance, although the output code is 00, it is invalid. From the truth table, we also recognize that the priority order of the inputs from high to low is I_3, I_2, I_1, I_0. Therefore, if I_3 and I_2 are both "1", only I_3 is encoded.

According to Table 1, the output expressions of the priority encoder are written as

$$\begin{cases} Y_1 = I_3 + I_2, \\ Y_0 = I_3 + \overline{I_2} I_1, \\ GS = \overline{I_3 I_2 I_1 I_0}. \end{cases} \tag{1}$$

From eq. (1), we see that the priority encoder is mainly made up of logic OR and AND functions. However, the OR logic contained in Y_1 and Y_0 cannot be obtained by coupling the items on the right of the expressions directly because there might be an identical bit "1" in different inputs that will induce multilevel intensities in the outputs Y_1 and Y_0. Apart from this, at least two SOAs are required to achieve Y_0. One is used to obtain $\overline{I_2} I_1$ and the other is used to obtain $I_3 + \overline{I_2} I_1$. GS is also difficult to obtain using an AND gate because there are too many inputs. To avoid multilevel intensities, reduce the number of SOAs and avoid using AND logic for multiple inputs, the expressions are modified as

$$\begin{cases} Y_1 = I_3 + \overline{I_3} I_2, \\ Y_0 = I_3 + \overline{I_3}\,\overline{I_2} I_1 \\ \quad = I_3 + \overline{(I_3 + I_2)} I_1, \\ GS = \overline{I_3 + I_2 + I_1 + I_0}. \end{cases} \tag{2}$$

As shown in eq. (2), Y_1 and Y_0 are never multilevel because of the simultaneous existence of I_3 and $\overline{I_3}$, which cannot be "1" at the same time. Thus, Y_1 and Y_0 are easily realized by coupling the items on the right of the expressions directly. $\overline{I_3}\,\overline{I_2} I_1$ (in Y_0) and GS are modified to $\overline{(I_3 + I_2)} I_1$ and $\overline{I_3 + I_2 + I_1 + I_0}$ respectively because the realization of the NOR gate in the SOA is much easier than that of the AND gate.

The system configuration is illustrated in Figure 1. Regarding Y_1, the intensity of the probe light I_2 is modulated by the intensity of the pump light I_3 according to the XGM effect in the SOA. When I_3 is strong (high level), carriers in SOA1 are heavily consumed and SOA1 becomes saturated. Thus, I_2 cannot be amplified and the output is "0". On the contrary, when I_3 is weak (low level), almost no carriers in SOA1 are consumed and I_2 is amplified. Therefore, the logic operation $\overline{I_3} I_2$ is easily obtained at the output of SOA1 when the average power of I_3 is much greater than that of I_2. Y_1 can then be achieved by coupling $\overline{I_3} I_2$ and I_3 directly. As for Y_0, both I_3 and I_2 act as pump lights with nearly the same power, and I_1 serves as the probe light. With a similar operation principle, SOA2 becomes saturated as long as either I_3 or I_2 is high, and I_1 is suppressed accordingly. Only when both I_3 and I_2 are low is I_1 amplified. Hence, we obtain $\overline{(I_3 + I_2)} I_1$, and Y_0 is demonstrated by combining $\overline{(I_3 + I_2)} I_1$ and I_3. While the pump lights I_3, I_2, I_1 and I_0 are co-propagated with another continuous-wave (cw) probe

Table 1 Logic truth table for an all-optical digital 4-bit priority encoder

Input				Output		
I_3	I_2	I_1	I_0	Y_1	Y_0	GS
0	0	0	0	0	0	1
0	0	0	1	0	0	0
0	0	1	×	0	1	0
0	1	×	×	1	0	0
1	×	×	×	1	1	0

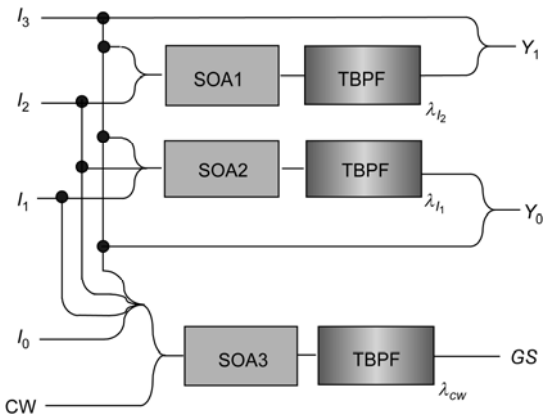

Figure 1 System configuration.

light, the logic NOR gate for multiple inputs can be realized and the warning output GS is achieved.

2 Experimental setup and results

The experimental setup for the all-optical digital 4-bit priority encoder is depicted in Figure 2. The cw beams generated by LD1, LD2, LD3, LD4 and LD5 have wavelengths of 1560.75 (λ_{I_3}), 1557.69 (λ_{I_2}), 1554.45 (λ_{I_1}), 1551.24 (λ_{I_0}) and 1547.72 nm (λ_{cw}), respectively. The data signals at wavelengths from λ_{I_3} to λ_{I_0} are modulated simultaneously by two Mach–Zehnder modulators (MZMs) to produce RZ signals at 40 Gbit/s with a duty cycle of 33%. The fixed data stream "1001 0011 0101 0010" is provided by the bit pattern generator (BPG). An erbium-doped fiber amplifier (EDFA) is exploited to amplify the signals to 15.63 dBm. The four data signals are then separated by a wavelength- division demultiplexer (WDM) with channel spacing of 1.6 nm. The signals at λ_{I_2}, λ_{I_1} and λ_{I_0} are delayed with different bit time durations by optical delay lines (ODLs) to emulate four different data signals I_3, I_2, I_1 and I_0.

The corresponding absolute data sequences are "1001 0011 0101 0010", "0101 0010 0110 1010", "0100 1010 0100 1101" and "1010 1001 0100 1001". Their temporal waveforms and eye diagrams are recorded by the communication signal analyzer (CSA). The eye diagrams are measured for 2^7–1 pseudo-random binary sequence input. I_3 is divided between two paths, one to combine with the SOA1 (CIP ultrafast SOA) output, and the other as one input of SOA1; the average powers are –6.12 and 10.35 dBm, respectively. I_2 is attenuated to –8.96 dBm as the probe light. SOA1 is biased at 250 mA with a recovery time of about 50 ps. The 3-dB bandwidth of the bandpass filter (TBPF) after SOA1 is 1 nm, which ensures the pulse width of the output

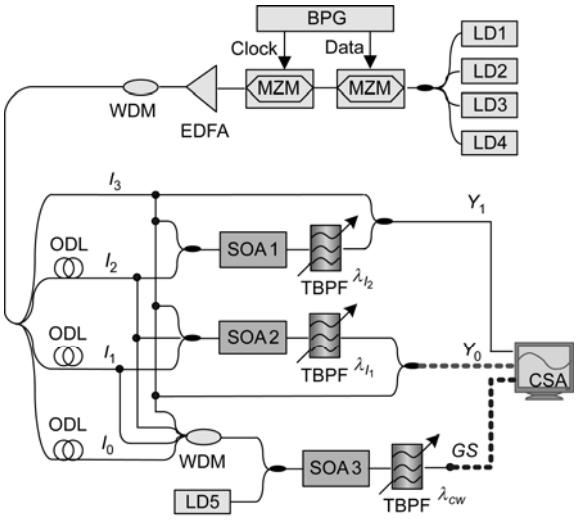

Figure 2 Experimental setup for the 4-bit all-optical digital priority encoder.

$\overline{I_3}I_2$ is not too wide. The TBPF central wavelength is detuned with a slight blue shift from λ_{I_2} to improve the quality of the final logic signal and increase the operation speed. Y_1 is then achieved by coupling $\overline{I_3}I_2$ and I_3 directly.

Similarly, as for $\overline{(I_3+I_2)}I_1$, the average power of the SOA2 inputs, I_3, I_2 and I_1, are adjusted to 6.60, 6.45 and –8.47 dBm, respectively. Y_0 is demonstrated by combining $\overline{(I_3+I_2)}I_1$ and I_3, and the TBPF is a little blue shifted from the signal light at λ_{I_1}. The cw light generated by LD5 serves as the probe light of SOA3 with power of –7.72 dBm. The pump light is composed of I_3, I_2, I_1 and I_0, whose average powers are 5.27, 7.54, 10.12 and 8.99 dBm, respectively. The cw light is filtered out by the TBPF at the output port of SOA3, which provides the warning signal *GS*.

The temporal waveforms and eye diagrams are illustrated in Figure 3. Figures 3(a)–(d) show the original input data of the input signals. The zero levels of $\overline{I_3}I_2$ and $\overline{(I_3+I_2)}I_1$, as shown in Figure 3(e) and (f) respectively, are not so flat because the gain of the probe light is not compressed completely. The final output items Y_1 and Y_0 are depicted in Figure 3(g) and (h), respectively. Both are of higher quality than the intermediate results $\overline{I_3}I_2$ and $\overline{I_3}\,\overline{I_2}I_1$ since the original signal is used. The *GS* output is shown in Figure 3(i).

Theoretically, *GS* should be a dark RZ format because the probe light is a continuous wave. However, owing to the heavy consumption of the carriers in the SOA when there are two, three or four "1" bits in the coupled input signals, as well as the carrier density recovery not being fast enough, a series of small ripples are present at the positions of "0" bits. For the same reason, the "1" bits, whose pulse width should be very wide, are suppressed by the next input pulse when they have not fully recovered. Consequently, the final output *GS* is in the form of a RZ signal with a little broadening. Although the *GS* data stream is not a perfect RZ signal, its temporal logic levels still satisfy the designed logic function.

Figure 4 shows the measured extinction ratios and eye opening factors of all logic units. All extinction ratios exceed 10 dB, and the eye opening factors exceed 0.7. This scheme has the potential to operate at a higher bit rate because wavelength conversion with a similar program was demonstrated at 320 Gb/s [12,13].

3 Conclusion

The all-optical digital 4-bit priority encoder based on RZ signals at 40 Gbit/s was proposed and experimentally demonstrated employing the XGM effect in SOAs cascaded with detuning bandpass filters. As the final results, correct and clear temporal waveforms and open eye patterns were

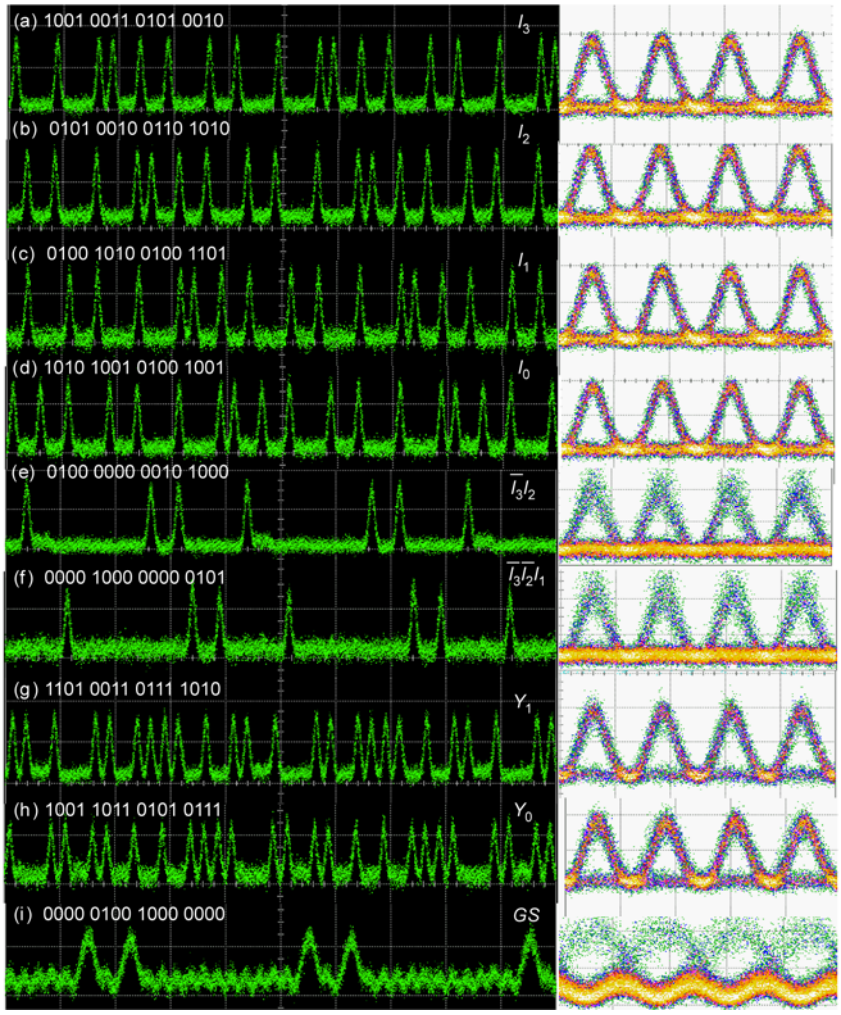

Figure 3 Temporal wave forms and eye diagrams of all logic units. (a)–(d) Original inputs; (e),(f) intermediate results; (g)–(i) final encoding outputs.

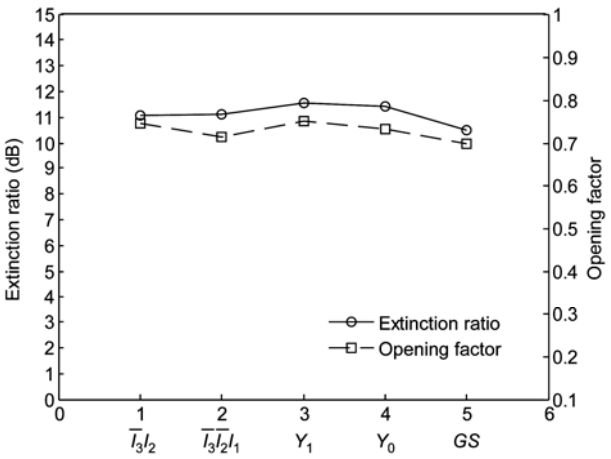

Figure 4 Extinction ratios and opening factors of all logic units.

obtained, and extinction ratios exceeding 10 dB were achieved. A more complicated digital priority encoder circuit with a higher operation bit rate could be realized by cascading the 4-bit priority encoder. Moreover, the proposed scheme has the potential to be large-scale integrated.

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