J Sign Process Syst (2014) 76:223–224
DOI 10.1007/s11265-014-0930-z

Latest Advances on Design and Implementation of DSP Systems

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Published online: 24 July 2014

New challenges for implementations and design methodologies have been introduced over the years and the trend seems to continue. More and more complex algorithms need to be implemented with higher performance but with strict constraints on power consumption. There is need for improving the implementation techniques, design methodologies, and algorithm-architecture optimizations to tackle the challenges in present signal and information processing systems. This special issue contains a selection of papers reporting the latest advances on design and implementation of signal processing systems. The topics span from circuit level architectures in memories and arithmetic to dynamic code generation and from application implementations on mobile devices or heterogeneous platforms.

In their paper *Improving the Reliability of MLC NAND Flash Memories through Adaptive Data Refresh and Error Control Coding*, Yang, Chen, Mudge, and Chakrabarti propose a combination of data refresh policies and low cost error control coding (ECC) schemes to address the errors in multi-level cell (MLC) NAND Flash memories given application characteristics. It is shown that an appropriate choice of refresh interval and BCH based ECC scheme can minimize memory energy while satisfying the reliability constraint.

Hardware implementation of associative memories based on message passing algorithms on sparse graphs is described in *Algorithm and Architecture of Fully-Parallel Associative Memories Based on Sparse Clustered Networks* by Jarollahi, Onizawa, Gripon, and Gross. Architectures are derived that eliminates the need for computationally-complex winner-take all circuits. This results in improvement in clock frequency by about a factor of 2 and a reduction in circuit size. A design space exploration is provided and hardware complexity of the FPGA implementations are described.

Antao and Sousa propose an implementation of an arithmetic accelerator for modular arithmetic based on the residue number system (RNS) in their paper *A Flexible Architecture for Modular Arithmetic Hardware Accelerators based on RNS*. An architecture of processing elements connected as a ring is proposed. The architecture is fully-parallel and is scalable to different algorithms and operand sizes. Implementations on FPGAs are provided.

A Real-time Scalable Object Detection System using Low-Power HOG Accelerator VLSI by Takagi, Tanaka, Izumi, Kawaguchi, and Yoshimoto proposes a real-time object detection system using a Histogram of Oriented Gradients (HOG) feature extraction accelerator and reconfigurable multiply-accumulate array for supporting processing objects of different shapes. The proposed approach uses support vector machine for early classification. The system has been implemented on a 65 nm CMOS technology and the characteristics of the chip are reported in the paper.

Blake and Hunter propose dynamically generated code for fast Fourier transforms. The fastest Fourier Transform in the South (FFTS) is a discrete Fourier transform library for x86 and ARM based devices, which was shown to be faster than FFTW, Intel IPP and Apple vDSP partly due to the use of program specialization and dynamic code generation. In this work, FFTS has been modified to dynamically exploit streaming store instructions on x86 machines, resulting in speedups of over 10 %, Also, when dynamic code generation is prohibited on some mobile platforms, FFTS has been altered to avoid it, while maximizing the performance.

In paper *Computer Vision Accelerators for Mobile Systems based on OpenCL GPGPU Co-Processing*, Wang, Xiong,

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Yun, and Cavallaro describe an implementation of image inpainting-based object removal algorithm on a heterogeneous mobile platform. The application is partitioned to be executed both on CPU and GPU. The experiments show significant speed-up compared to single thread CPU execution. The paper studies also implementation trade-offs and optimization strategies for increasing the performance.

Jayaprasad, Kirkko-Jaakkola, Collin, and Takala propose a novel method for three-dimensional navigation and localization of a land vehicle in a multi-storey parking-garage in their paper *Indoor Localization Methods Using Dead Reckoning and 3D Map Matching*. The solution uses low-cost gyro and odometer with additional information from a 3D map. The map matching based on particle filtering and collision detection techniques are used to determine the location of the vehicle in a building. The proposed approach is extended with non-stationary 3D maps.

We would like to thank all of the authors of this special issue for their contributions. We also thank the anonymous reviewers for their efforts in ensuring the quality of the papers. We also extend our appreciation to C. Clark for her help on setting up this issue. We hope that you enjoy the special issue and find the articles informative and useful.

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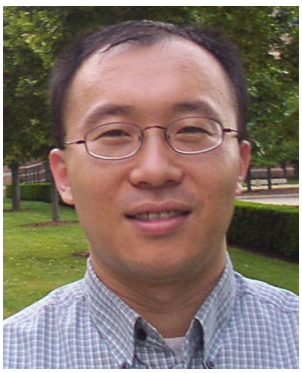

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