J Electron Test (2016) 32:405–406
DOI 10.1007/s10836-016-5608-y

Guest Editorial: Analog, Mixed-Signal and RF Testing

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Received: 2 July 2016 / Accepted: 2 July 2016 / Published online: 18 July 2016

Analog, Mixed-Signal and Radio-Frequency circuits represent a small fraction of the total volume of semiconductor production. However, they pose very specific challenges and headaches – more often than not – to both design and test engineers. For complex systems, the costs of AMS-RF test and test development can lead to a bottleneck in industrialization of a product.

This is the reason why a rather small but active community meets on a yearly basis at the International Mixed-Signal Testing Workshop (IMSTW). In 2015 the workshop was held in Paris and brought a number of interesting proposals to public discussion. As program chairs of IMSTW, we decided to invite submissions for a JETTA special issue with a call-for-papers open to contributions reaching beyond the workshop community. Therefore, some papers in this special issue are extended versions of IMSTW papers and others are new contributions.

The first three papers deal with Built-in-Self Test (BiST). The paper by Renaud et al. discusses the details of a switched-capacitor ramp generator for static testing of high performance ADCs. This ramp generator is shown to test a Pipeline ADC with a reduced-code strategy that requires only 6 % of the total number of codes. The second paper, contributed by Roberts et al., presents a complete scheme of injecting and analyzing jitter in high-speed I/Os. Software-generated Sigma-Delta bit-streams are stored in on-chip cycling registers and processed by amplitude-mode or time-mode filters in order to provide robust stimulus. The signature extraction part of the BiST requires only a comparator and a few logic gates. Finally, Bashir et al. describe in the third paper a built-in measurement mechanism to evaluate the degradation due to injection pulling in a Digital-to-Frequency Converter. In order to minimize the injection pulling effect, the authors introduce a programmable delay line in the circuit. Thus, the BiST hardware is used for both improving and testing device performance.

IMSTW 2015 had significant contributions from the production test development community. The fourth paper in this special issue of JETTA, contributed by Leisenberger and Schatzberger, is a representative and develops a contact screening procedure for EEPROM memories. Due to high density requirements, single via contacts are used in memory arrays and this poses reliability issues. It is shown that high-resistive contacts are prone to lift-off failure but are not detected by conventional tests. Hence, an improved measurement procedure is proposed that exploits Design-for-Test modifications in the memory array.

The third category gathers four papers that deal with reliability, diagnosis and machine-learning. The fifth paper of this special issue, by Yu et al., presents a statistical framework for fault diagnosis, which is based on a combination of tools: Extreme Learning Machine for the model and a Firefly algorithm for optimization (an evolutionary method, like particle swarm, where the random generation is replaced by a more efficient chaotic map). The sixth paper also deals with diagnosis but in a much different framework. The purpose of Oliveira and Machado da Silva is to identify hardware faults in a health monitoring system. They rely on a fuzzy logic system to devise whether abnormal sensor data

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readings are due to a system failure or a severe health issue. In the seventh paper, Lin et al. use a Perceptron Neural Network in order to learn the non-linear relationship between circuit parameters of a power amplifier and the atomic flux divergence in the metal interconnect. This metric can be related to electromigration-induced reliability degradation. The primary target of the paper is to understand the mechanisms in order to harden the circuit. Indeed, the Neural Network is used to find optimal circuit parameter values (from a reliability point of view) at a fraction of the computational cost that would be required by an optimization based on Finite Element Modeling. The eighth and last paper is also related to reliability, but in a much different way. Uygur and Sattler show how specific fingerprint models can be developed that perfectly match the circuit structure to the functional specification, which greatly facilitates verification including the verification of Design-for-Test functionalities.

Before closing this note, we want to greatly thank the authors who decided to submit their works to this special issue. We are particularly grateful to the reviewers without whom it would be impossible to reach the high quality level demonstrated by the papers in this special issue. We hope that the readers will enjoy it.

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