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Editorial

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This issue contains four papers and three *Letters*. The topics covered are contactless testing, soft errors, verification, RF test and aperiodic testing.

The first paper is on contactless testing of printed circuit boards (PCB). Authors are Renbi and Delsing from Luleå University of Technology, Sweden. A companion paper by the same authors introducing this topic appeared in the last issue with the title, "Contactless Testing of Circuit Interconnects," *JETTA*, volume 31, number 3, pp. 229–253, June 2015. The paper in this issue documents a case study of testing printed circuit boards with ball grid array (BGA) packages.

The second paper describes a latch designed for tolerance of single event upsets (SEU). The authors, Huang and Liang from Hefei University of Technology, Hefei, China, and Hellebrand from University of Paderborn, Paderborn, Germany, use dual modular redundancy. They presented the idea of this design originally at the *Design*, *Automation and Test in Europe Conference* at Dresden, Germany in 2014.

The third paper addresses test generation for functional verification. The authors are Cruz, Fernández, Lozano, Salinas and Vargas of National Polytechnic Institute, Mexico City, Mexico. They convert the functional specification into a set of features referred to as coverage points. Their Compact-BinDE system for generating tests attains 99 % coverage of those points.

The fourth paper contributes an alternate test technique to assess the effects of process variation on an RF circuit. The circuit under test is a low noise amplifier (LNA) and a monitoring circuit, placed on the same chip but otherwise not connected to the LNA, is a dummy current mirror. Authors of this paper are Dimakos, Stratigopoulos and Mir from TIMA, 38,000 Grenoble, France, and Siligaris and De Foucauld from CEA-LETI, Grenoble, France. A preliminary version of this work was presented at the *19th IEEE International Mixed-Signal*, *Sensors*, *and Systems Test Workshop* at Porto Alegre, Brazil in 2014.

The first *JETTA Letter* is contributed by Wang, Liu, Chen, Bi, M.-L. Li and Y.-Q. Li from University of Saskatchewan, Saskatoon, Canada. The authors demonstrate the effectiveness of their patented sensor for detecting single-event transients by actually building the device and irradiating it by a laser.

In the second *Letter*, Gunasekar of Intel Corporation, Santa Clara, California and Agrawal from Auburn University, Auburn, Alabama present a linear complexity algorithm, called the *k*th-root solution, for deriving best clock frequencies to minimize the test time of power constrained test. An early version of this work was presented at the *28th International Conference on VLSI Design* at Bangalore, India in January 2015.

The authors of the third *Letter* are Simionovski and Wirth of Universidade Federal do Rio Grande do Sul (UFRGS), Porto Alegre, Brazil, and Vaz and Gonçalez from Instituto de Estudos Avançados (IEAv), São José dos Campos, Brazil. The topic is similar to the first letter. A built-in current sensor with dynamic storage cell, named DynBICS, is fabricated in IBM 130 nm technology and tested for high total ionizing dose (TID).

Finally, I would like to draw the attention of our readers to a correction to a recently published paper (*JETTA*, volume 30, number 6, pp. 653–663, December 2014) that appears at the end of this issue.

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