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Editorial

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This issue contains six papers and two *Letters*. The topics covered are printed circuit board test, functional verification, soft errors, mixed-signal test and measurement, network-on-chip testing, microfluidic device testing, and test generation complexity.

The first paper is on contactless testing of printed circuit boards (PCB). Authors are Renbi and Delsing from Lule University of Technology, Sweden. They address the problem of interconnect test on a PCB where feature size may be smaller than 10 μm. After a discussion of difficulties encountered in testing such interconnects, the authors propose a new method of contactless sensing using coupled striplines. The paper contains analysis, simulation and experiment.

The second paper is on high-level verification and comes from the program of the *IEEE Latin American Test Workshop* (LATW) of 2014. We are thankful to the Guest Editor, Leticia M. B. Poehls. The authors, Marquez, Strum and Chau from University of Sao Paulo, Brazil, adopt sequential equivalence checking for high level verification of functions.

The third paper addresses simulation of single event transients. The authors are Andjelković, Ristić and Jovanović from University of Niš, Serbia, and Petrović and Stamenković of IHP GmbH, Frankfurt, Germany. They show how the robustness of single event latchup protection logic can be evaluated and improved.

The fourth paper contributes a technique for estimating and correcting timing error in a time-interleaved analog to digital converter (ADC). Authors are Guo, Wang, Jiang and Qiu from University of Electronic Science and Technology of China, Chengdu, China.

The fifth paper optimizes the arrangement of modules of a network on chip for test using the IEEE 1149.1 boundary scan test standard. Test time is minimized while power is a constraint. This contribution comes from Fotovatikhah, Naraghi, Tavakoli and Ghadiry of Islamic Azad University, Arak, Markazi, Iran.

In the sixth paper the authors, Mukherjee of Techno India, Salt Lake, Kolkata, West Bengal, India and Samanta from Bengal Engineering and Science University, Shibpur, Howrah, West Bengal, India, discuss the design for testability and testing of microfluidic devices.

The first *JETTA Letter* is contributed by Das from Jadavpur University, Kolkata, India and Fujiwara from Osaka Gakuin University, Osaka, Japan. They define a class of sequential circuits, called max-testable, for which the complexity of test generation is similar to that for combinational circuits.

In the second *Letter*, Yu, Tian, Xu and Shi from Zhejiang University, Hangzhou, China present the design of a built-in capacitance measurement circuit.

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