J Electron Test (2012) 28:773–774
DOI 10.1007/s10836-012-5341-0

Editorial

Vishwani D. Agrawal

Received: 20 November 2012 / Accepted: 20 November 2012 / Published online: 30 November 2012

The *JETTA* Editorial Board meeting at Anaheim, California on November 7, 2012 was attended by (*left to right in the photograph, standing*) Michael Hsiao, Adit Singh, Haralampos Stratigopoulos, Patrick Girard, Erik Jan Marinissen, Hans Manhaeve (Guest Editor), Hans-Joachim Wunderlich, Kwang-Ting (Tim) Cheng, Shawn Blanton, Said Hamdioui, Mohammad Tehranipoor, Krishnendu Chakrabarty, Cheng-Wen Wu and Xiaowei Li, and (*sitting*) Nicola Nicolici, Charles Glaser (Springer), Sybille Hellebrand, Michel Renovell and Vishwani Agrawal. I will summarize the proceedings of the meeting in the next issue.

This issue of *JETTA* contains seven papers and three *Letters*. The topics covered are single event upset (SEU), electromagnetic compatibility, through silicon via (TSV) testing, network-on-chip (NoC) testing, application of zero-suppressed binary decision diagram (ZBDD) to path diagnosis, and mixed-signal test. The first four papers are derived from the *Twelfth IEEE Latin-American Test Workshop* (LATW), 2011, and the next two from the *Sixteenth IEEE European Test Symposium* (ETS), 2011.

The first paper describes an FPGA-based processor emulator that rapidly injects a large number of SEU-like faults. This hardware platform evaluates and helps optimize the robustness of the processor software implemented with embedded signature monitoring techniques. Authors are Portela-Garcia, Lindoso, Entrena, Garcia-Valderas and Lopez-Ongil from University of Madrid, Madrid, Spain, and Marroni, Pianta, Bolzani Poehls and Vargas from Catholic University of Rio Grande do Sul–PUCRS, Porto Alegre, Brazil.

V. D. Agrawal (✉)
Auburn University, Auburn, AL 36849, USA
e-mail: vagrawal@eng.auburn.edu

The second paper focuses on electromagnetic interference (EMI) effects on electronic devices, especially when they are aged. A direct power injection (DPI) procedure as specified by the IEC 62132-3 standard is used to assess the susceptibility of a phased-locked loop (PLL) circuit to EMI. Authors are Boyer, Ben Dhia and Lemoine from Université de Toulouse, Toulouse, France, Li from Chinese Academy of Sciences, Beijing, China, and Vrignon of Freescale Semiconductor, Toulouse, France.

The third paper studies the combined effects of EMI and ionizing radiation on electronic systems. The authors examined the behavior of matrix multiplication and other functions implemented on FPGA when executed in a radiation environment created in a laboratory. Useful observations about static and dynamic faults and power supply noise are reported. The paper is authored by Benfica, Bolzani Poehls and Vargas from Catholic University–PUCRS, Porto Alegre, Brazil, Lipovetzky, Lutenberg and García from Universidad de Buenos Aires, Buenos Aires, Argentina, Gatti from Instituto Nacional de Tecnología Industrial–INTI, Buenos Aires, Argentina, and Hernandez from Universidad ORT, Montevideo, Uruguay.

At the beginning of this year we published a special issue (*JETTA*, volume 28, number 1, February 2012) containing ten selected papers on testing of 3-D stacked devices. Several test problems need to be solved before benefits of the 3-D stacking can be realized. Prominent among these is testing of through-silicon vias (TSV) that transmit signals between the stacked chips. This is the topic of the fourth paper. Authors, Pasca, Anghel and Benabdenbi of TIMA Laboratory, Grenoble, France, propose a built-in self-test method for opens, shorts, delay faults and coupling faults of TSVs. Reconfiguration of the test hardware and reduction of test time are the main features of the proposed method.

Diagnosis of network on chips (NoC) is addressed in the fifth paper. Although testing is done for structural faults, the functionality of the interconnection switch is examined to determine whether a defective switch can still work perhaps with reduced performance. The authors are Dalirsani, Holst, Elm and Wunderlich from University of Stuttgart, Stuttgart, Germany.

The authors of the sixth paper, Neophytou of University of Nicosia, Nicosia, Cyprus, and Christou and Michael of University of Cyprus, Nicosia, Cyprus, revisit the problem of path diagnosis to analyze correlation (or common segments) among paths. Enumeration of segments that can apparently lead to high complexity is avoided by using a technique called the zero-suppressed binary decision diagram (ZBDD).

The seventh paper is on the mixed-signal test bus standard 1149.4 and is authored by Hannu, Häkkinen, Voutilainen, Jantunen and Moilanen from University of Oulu, Oulu, Finland. The standard that is now over a decade old provides for hardware test access to embedded mixed-signal components of a system. The paper outlines the requirements of the changing device technology and discusses suggested modifications of the standard.

In the first of three *letters*, Ruiz and Morata of Escuela Universitaria Salesiana de Sarriá, Barcelona, Spain, and Fernández-Garcia and Gil of UPC Barcelona Tech, Terrassa, Spain, demonstrate that the negative bias temperature instability (NBTI) in a CMOS ring oscillator circuit reduces the frequency and power consumption. In the second *letter*, Chakraborty of Lattice Semiconductor, Hillsboro, Oregon, and Agrawal of Auburn University, Auburn, Alabama, provide a MATLAB program to estimate the defect level from automatic test equipment (ATE) data. The third letter, authored by Ren, Fan and Chen from University of Saskatchewan, Saskatoon, Canada, Wen and Wong from Cisco Systems Inc., San Jose, California, van Vonno of Intersil Inc., Milpitas, California, and Witulski and Bhuva from Vanderbilt University, Nashville, Tennessee, analyze the influence of single-event transients on DC-to-DC converters.