J Electron Test (2011) 27:579
DOI 10.1007/s10836-011-5254-3

Editorial

Vishwani D. Agrawal

Received: 5 September 2011 / Accepted: 5 September 2011 / Published online: 13 September 2011
© Springer Science+Business Media, LLC 2011

This issue of *JETTA* contains eight papers including one *JETTA Letter*. The topics covered are design for testability, test data compression, mixed-signal test, fault-tolerance, interconnect testing, and testing of microfluidic circuits. The second paper is derived from the program of *IEEE European Test Symposium* (ETS) of 2010. The fourth and fifth papers had their initial presentations made at the *IEEE Latin-American Test Workshop* (LATW) of 2010. Cecilia Metra (ETS) and Fabian Vargas (LATW) once again deserve credit for the editing of these papers.

In the first paper, authors, Ooi from Universiti Teknologi Malaysia and Fujiwara of Osaka Gakuin University, Japan propose novel design for testability procedures. By incorporating a thru function that allows direct propagation of signals between flip-flops and a hold function they show reduction in test application time over full scan and reduction in test generation time over that for the unmodified sequential circuit.

The second paper aims at locating flip-flops capturing faulty data during scan test. In the proposed scheme, scan-out data is compacted through two compactors in space and time, respectively. As a result aliasing loss is significantly reduced. This work first appeared at the ETS 2010. The paper is authored by Benware, Mrugalski, Pogiel and Rajski of Mentor Graphics, USA, and Solecki and Tyszer of Poznań University of Technology, Poland.

Switched current is an emerging design methodology with perceived advantages, as explained in the third paper, over the prevailing switched capacitor implementations of mixed-signal or analog circuits. Authors Jierong, Yigang and Meirong of Hunan University in China describe a method for testing switched current circuits.

V. D. Agrawal (✉)
Auburn University,
Auburn, AL 36849, USA
e-mail: vagrawal@eng.auburn.edu

The fourth article experimentally examines the fault-tolerant behavior of triple modular redundancy (TMR) used in a single-event upset (SEU) environment. The authors, Foucard, Peronnard and Velazco of Laboratoire TIMA, France, first presented this work at LATW 2010. The results identify a weakness of the TMR due to the lack of redundancy in the majority voter circuit. A modification, termed X-TMR, is shown to have higher fault-tolerance. Unfortunately, the paper lacks relevant details of the X-TMR design.

The fifth and sixth papers discuss interconnect testing. Hervé and Moraes of CEITEC S.A., Brazil, and Almeida, Lubaszewski, Kastensmidt and Cota of Universidade Federal do Rio Grande do Sul, Brazil initially presented their work at LATW 2010. Their paper discusses functional test of interconnects in a network on chip. In the next paper, Zhu, He, Wu and Pan of Tsinghua University, China present a method of reconfigurable test points to test interconnects in a field programmable gate array (FPGA).

Testing of microfluidic devices is the topic of the seventh paper. The microfluidic technology has been used to construct biochips with applications in medicine. The paper is authored by Mitra of National Institute of Technology, Durgapur, India, Ghoshal and Rahaman of Bengal Engineering and Science University, Sibpur, India, Chakrabarty of Duke University, USA, and Bhattacharya of Indian Statistical Institute, Kolkata, India. The proposed test consists of a droplet taking an Euler tour through the interconnects of the device under test.

The final article is a *JETTA Letter* authored by Kavithamani and Manikandan of Coimbatore Institute of Technology, India and Devarajan of Government College of Technology, Coimbatore, India. They propose testing of an analog circuit by determining the locations of poles of the transfer function in the complex frequency plane through measurements. Acceptable deviations of poles corresponding to the tolerance range of component values are pre-calculated by Monte Carlo simulation.